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VLSI Based Design of Low Power and Linear CMOS Temperature Sensor

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Abstract— Complementary Metal Oxide Semiconductor (CMOS) temperature sensor is introduced in this paper which aims at developing the MOSFET as a temperature sensing element operating in sub-threshold region by using dimensional analysis and numerical optimization techniques A linear CMOS temperature to voltage converter is proposed which focuses on temperature measurement using the difference between the gate-source voltages of transistors that is proportional to absolute temperature with low power. This proposed CMOS temperature sensor is able to measure the temperature range from 0^oC to 120^oC . A comparative study is made between the temperature sensors based on their aspect ratio under the implementation of UMC 180nm CMOS process with single rail power supply of 600mV.

Keywords– Aspect ratio , CMOS-Complementary Metal Oxide Semiconductor, MOSFET-Metal Oxide Semiconductor Field Effect Transistor, Sub-threshold ,Temperature sensor, Low power , Linearity.

INTRODUCTION

An important issue for powerful, high-speed computing systems (containing microprocessor cores and high speed DRAM) is thermal management. This is of special concern with laptops and other portable computing devices where the heat sinks and/or fans can only help dissipate the heat to a limited degree. This makes variations in clock frequency and/or variation in modes of device operation for DRAM, Flash, and other systems necessary. On-chip smart CMOS temperature sensors have been commonly used for thermal management in these applications. The main considering factors of temperature sensor are as follow:

Power : In VLSI implementation many small devices are incorporated resulting into higher and higher level of integration causing too much of heat dissipation. So there is a need of reducing power and thereby also reducing the production cost. For this purpose the power consumption must be in nanowatt.

Area : Series connected MOSFET's used for current sink increases the die area of the design, also the sizing of transistor plays an important role in deciding the chip area. The area should be small approximately $0.002m^2$.

Start-up circuit: Start-up circuit is required in the design if the transient response of the sensor takes a significant amount of time in reaching the steady state. If steady state time is less than 200ms in the worst case then it eliminates the necessity to start-up circuit.

As the CMOS technology scales down, the supply voltage also scales down from one generation to the next. It becomes difficult to guarantee that all the transistors work in saturation as the supply voltage drops.Therefore, the traditional temperature sensor configuration is not suitable for ultra low voltage applications for that reason the sensor should incorporate some modifications. This modification can be brought by making MOS transistors to work in sub-threshold region.

This paper presents a nanoWatt integrated temperature sensor for ultra-low power applications such as battery powered portable devices are designed and simulated using Cadence analog and digital system design tools UMC 180nm CMOS technology. Ultra-low power consumption is achieved through the use of sub-threshold (also known as weak inversion) MOS operation. The transistor are used in this domain because the current here is exponentially dependent on the control voltages of the MOSFET and they draw small currents so as to reduce power consumption. The sensor sinks current in nano-amperes from a single power supply of 0.6V and its power consumption is in nanoWatt . The performance of the sensor is highly linear in the range of 0–120 ^0C.

PROPOSED SCHEME

The proposed CMOS temperature sensor as shown in Fig 1 consists of main three blocks:

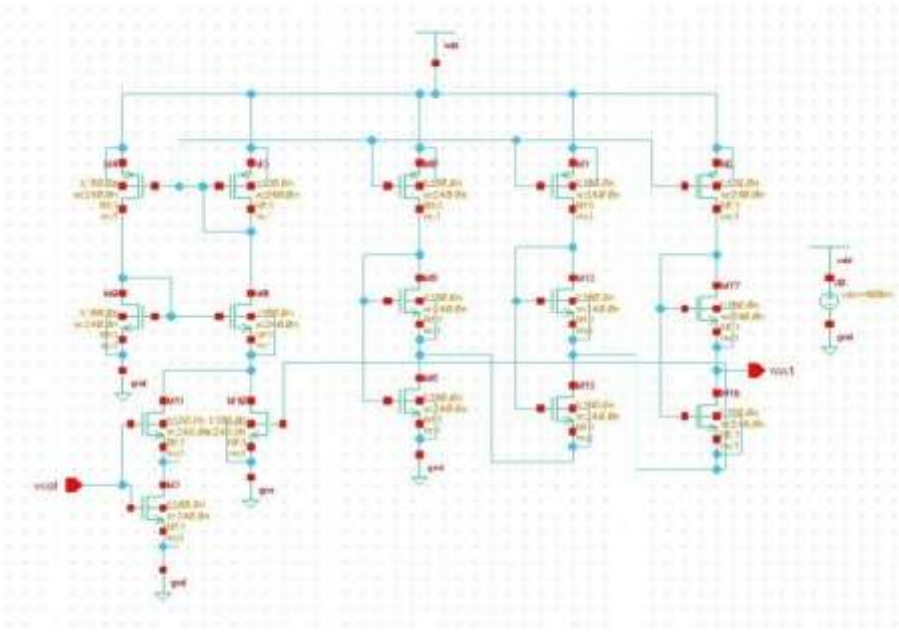


Fig 1. Circuit diagram of CMOS temperature sensor

(i) Current source sub-circuit: Analog circuits incorporate current references which are self biasing circuit . Such references are dc quantities that exhibit little dependence on supply and process parameters and a well defined dependence on the

(ii) Temperature variable sub-circuit: The temperature variable sub-circuit consists of three couples of serially connected transistors operating in sub-threshold region. It accepts current through PMOS current mirrors current mirror which gives a replica (if necessary, attenuated or amplified) of a bias or a signal current and produces an output voltage proportional to temperature.

(iii) One point calibration sub-circuit: Calibration consists of determining the indication or output of a temperature sensor with respect to that of a standard at a sufficient number of known temperatures so that, with acceptable means of interpolation, the indication or output of the sensor will be known over the entire temperature range of use. After packaging, the sensor is calibrated by measuring its die temperature at reference point using on-chip calibration transistors.

METHODOLOGY

The sub-threshold drain current I_D of a MOSFET is an exponential function of the gate-source voltage V_{GS} and the drain source voltage V_{DS}, and given by[8]:

$$I_D = KI_0 exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \times 1 - exp\left(\frac{-V_{DS}}{V_T}\right), \qquad (1)$$

Where

$$I_0 = \mu C_{OX}(\eta - 1) \times V_{T,}^2 \qquad (2)$$

and K is the aspect ratio (=W/L) of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_T is the thermal voltage V_{TH} is the threshold voltage of a MOSFET, and η is the sub-threshold slope factor.

In the current-source sub-circuit, gate-source voltage V_{GS9} is equal to the sum of gate-source voltage V_{GS8} and drain source voltage V_{DS10}:

$$V_{GS9} = V_{DS10} + V_{GS8} \quad (3)$$

$$V_{DS10} = V_{GS9} - V_{GS8} = \eta V_T \, In\left({}^{K_8}/_{K_9}\right) \quad (4)$$

M_{10} is operated in the sub-threshold region, so trans-conductance G_{DS10} is obtained by using Eqs. (1) and (4)

$$G_{DS10} = \frac{\partial I_{DS\,10}}{\partial V_{DS\,10}} = \frac{K_{10} I_0}{V_T} exp\left(\frac{V_m - V_{TH\,10}}{\eta V_T} - \frac{V_{DS\,10}}{V_T}\right) \quad (5)$$

$$I = V_{DS10} \times G_{DS10}$$

$$= \eta K_1 I_0 \left(\frac{K_9}{K_8}\right)^{\eta} \left(In\left(\frac{K_8}{K_9}\right)\right) exp\left(\frac{V_m - V_{TH\,10}}{\eta V_T}\right) \quad (6)$$

As M_{10} operates in sub-threshold region (V_m - V_{TH10}<0), I is increased by temperature, so the highest power consumption is in the upper temperature limit .Choosing the maximum current is a tradeoff between power consumption and linearity that can be obtained by simulation. In the temperature variable sub-circuit, as M_5, M_6, M_{15}, M_{12}, M_{16},M_{17} are in sub-threshold region, the relation between gate to source voltage and MOS current is equal to Eq. (4). According to Fig.1, currents of M_5, M_{12}, M_{16}, M_{17} are I and currents of M_6 and M_{15} are 3I and 2I . The transistor sizes in our design are simple having the same aspect ratio.

$$V_{OUT} = V_{GS6} - V_{GS5} + V_{GS15} - V_{GS12} + V_{GS16} - V_{GS17} \quad (7)$$

By using Eq. (4) with regard to currents of MOSFETs,output voltage is given by:

$$V_{OUT} = \eta V_T \, In\left(\frac{I_{D6} I_{D15} I_{D16} K_5 K_{12} K_{17}}{I_{D5} I_{D12} I_{D17} K_6 K_{15} K_{16}}\right) + \Delta V_{TH} \quad (8)$$

By replacing the currents of transistors, output voltage is obtained by:

$$V_{OUT} = \eta V_T \, In\left(\frac{6 K_5 K_{12} K_{17}}{K_6 K_{15} K_{16}}\right) + \Delta V_{TH} \quad (9)$$

By combination of Eqs. (7) and (9) output voltage can be obtained:

$$V_{OUT} = \frac{\eta K_B T}{q} \, In\left(\frac{6 K_5 K_{12} K_{17}}{K_6 K_{15} K_{16}}\right) + \Delta V_{TH0} = A \times T + B \quad (10)$$

where T is absolute temperature, A and B are temperature independent constants. Eq. (10) shows a linear relationship between absolute temperature and output voltage as depicted in Fig 3. Based on aspect ratio (W/L), temperature sensor is designed into two ways:

(i) Temperature sensor based on designed W/L ratio : In this design all the MOS transistors used in the circuit diagram are of different width and length. By using large length transistors ($L_{M6\text{-}11} >> L_{min}$) the sensitivity to the geometric variations can be minimized and an accurate temperature coefficient is expected. Large transistors also help to reduce the impact on threshold voltage due to random doping fluctuations. Different values of W/L ratio for corresponding MOS transistors is given in the Table I.

(ii) Temperature sensor based on minimum W/L ratio : In this design all the MOS transistors used in the circuit diagram are of same width and length. By minimum technology parameter it indicates that width(W) of transistor is 240nm and length(L) of transistor is 180nm. So the equation (10) becomes $V_{OUT} = \frac{\eta K_B T}{q} \, In(6) + \Delta V_{TH0} = A \times T + B.$

Table I Size of transistors

Transistor	**W/L (µm/µm)**
M_1	1 × (1.5/20)
M_2	10 × (3/3)
M_3	4 × (3/3)
M_6, M_8 , M_{10}	1 × (1/3)
M_7	3 × (3/3)
M_9	4 × (3/3)
M_{11}	28 × (3/3)
M_4, M_5, M_{12-14}	1 × (3/10)
M_{C1}, M_{C2}	1 × (1/20)

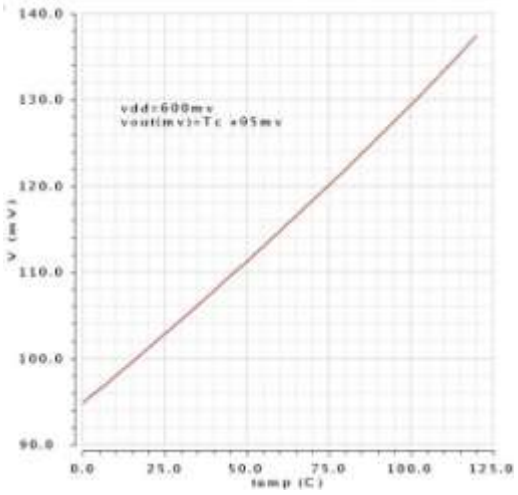


Fig 2.The linear relationship of output voltage and temperature of a

of a temperature Sensor based on designed W/L

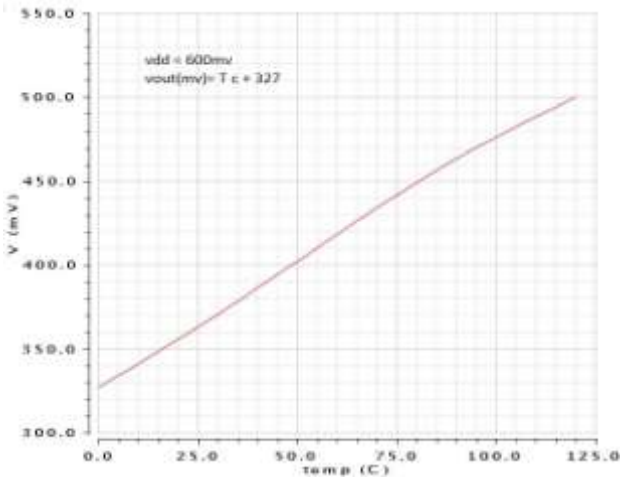
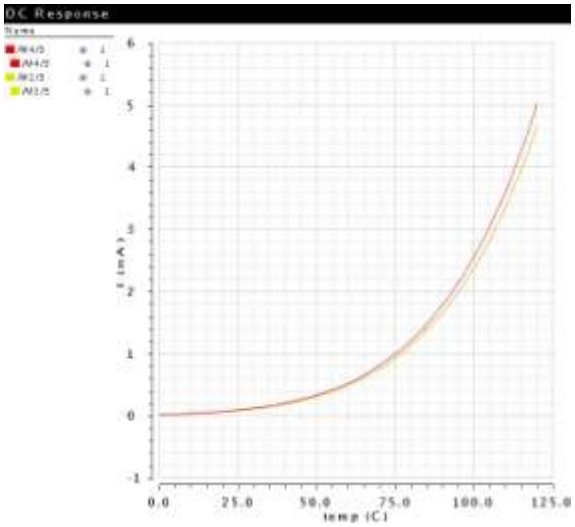


Fig 3. The linear relationship of output voltage and temperature

Temperature Sensor based on minimum W/L .



Sink current versus temperature graph for minimum W/L sensor

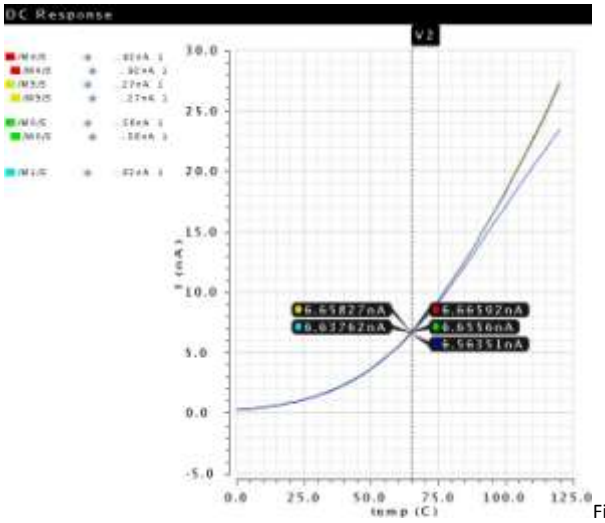


Fig 5. Sink current versus temperature graph for designed W/L sensor

Fig 4.

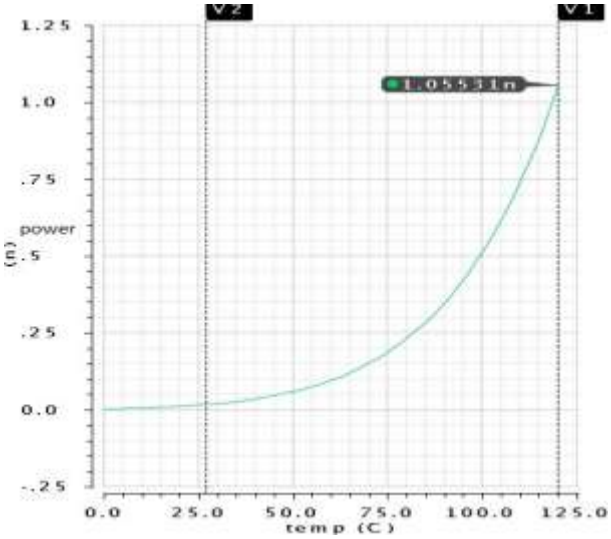


Fig 6. Power versus temperature graph for Temperature Sensor based on designed W/L

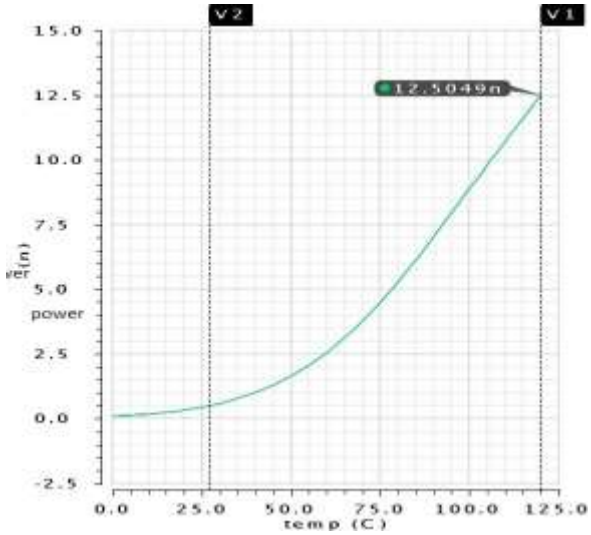


Fig 7. Power versus temperature graph for Temperature Sensor based on minimum W/L

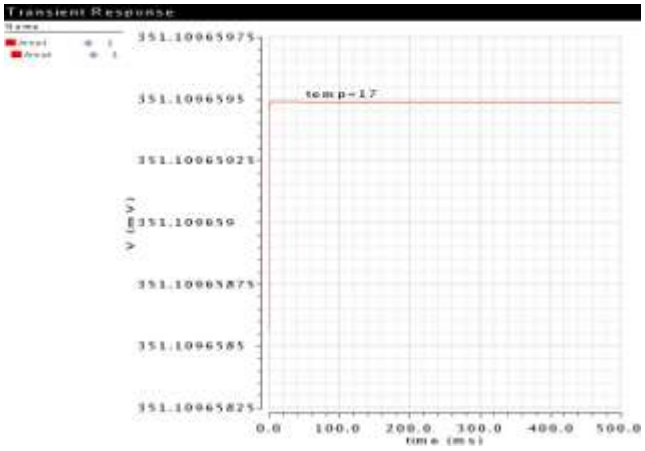


Fig 8. Transient response of designed W/L sensor at temperature 17^{0}C

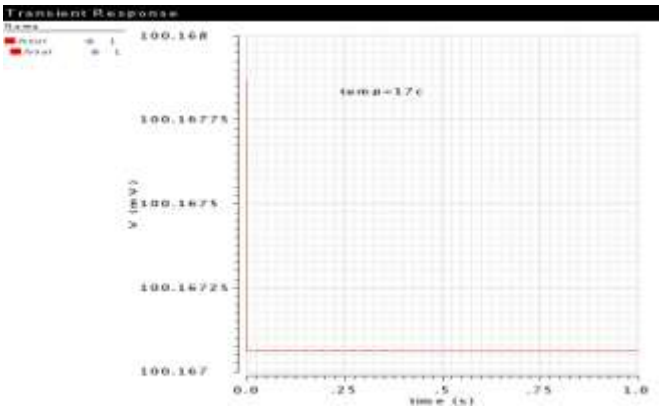


Fig 9. Transient response of minimum W/L sensor at temperature 17^{0}C

Table II Comparison of temperature sensor with previous works

Sensor	Power supply	Power cons.	Temp. range	Inaccuracy	Process
[1]	0.5, 1 V	119 nW	-10–30 ˚C	-0.8 to +1 ˚C	180 nm CMOS
[2]	–	38.5 µW	–	±2 ˚C	65 nm CMOS
[3]	2.7–5.5 V	429 µW	-50–125 ˚C	±0.5 ˚C	0.5 µm CMOS
[4]	1V	220 nW	0–100 ˚C	-1.6 to +3 ˚C	180 nm CMOS
[5]	3.0–3.8 V	10 µW	0–100 ˚C	-0.7 to +0.9 ˚C	0.35µm CMOS
[6]	1V	25 µW	+50–125 ˚C	-1 to +0.8 ˚C	90 nm CMOS
[7]	–	8.6 µW	-55–125 ˚C	±0.4 ˚C	160 nm CMOS
[8]	0.6–2.5 V	7 nW	+10–120 ˚C	±2 ˚C	180 nm CMOS
[This work designed W/L]	0.6–2.5 V	12.5nW	0–120 ˚C	±3 ˚C	180 nm CMOS
[This work minimum W/L]	0.6–2.5 V	1.05nW	0–120 ˚C	±6–7 ˚C	180 nm CMOS

SIMULATION RESULTS AND DISCUSSION

A linear temperature sensor that incorporates semiconductor devices and is capable of high accuracy over a very wide temperature range, such that the voltage drop varies approximately linearly in negative or positive dependence on temperature. The linear relationship of output voltage and temperature at a supply voltage of 600mV is shown in Fig 2 and Fig 3.Temperature Sensor based on

designed W/L sinks upto 28nA from a wide range of temperature with a V_{DD} of 600mV is given in Fig 5. As sink current is exponentially increasing with temperature its power consumption also increases. The overall power consumption is more of this temperature design as compared to temperature sensor based on minimum W/L ratio as shown in Fig 4.As the temperature is increased power consumed by the sensor also increases. The power consumption is of merely 12.5nW at 120^0C is shown in Fig 7.The power consumed is more by this sensor as compared to temperature sensor based on minimum W/L given in Fig 6.At temperature of 15^0C sustained oscillations are obtained in case of designed aspect ratio temperature sensor, at temperature of 17^0C smooth response is obtained spontaneously shown in Fig 8 and further on increasing the temperature oscillations are dominant. This proves temperature of 17^0C is the best temperature for transient response. In case of minimum aspect ratio temperature of 17^0C is the suitable temperature for transient response given in the Fig 9. The transient response of temperature sensor based on designed W/L is more practically realizable (similar to unit step response) as compared to temperature sensor based on minimum W/L .

CONCLUSION

This research investigate an ultra low power temperature sensor. Tables II and III shows the comparison between the designed sensor with previous works and its performance summary. As the oscillations were profound in the transient response of the temperature sensor, this can be eliminated by using Proportional Integral Derivative controller based on IMC approach so as to get smooth steady state response at a particular temperature. This transient response is helpful in determining the need of start-up circuit. It is required that if steady state time is less than 200ms then there is no need of start -up circuit. As a result, the temperature sensor based on two approaches of aspect ratio are significantly important according to their performances in relative desired characteristics. The layout area of the sensor is shown in the Fig 10 and Fig 11. From area and power point of view temperature sensor based on minimum aspect ratio is preferred whereas considering linearity, temperature error inaccuracy and transient response temperature sensor based on designed aspect ratio is dominant.

Table III Performance Summary

Parameter	temperature sensor based on designed W/L Value	temperature sensor based on minimum W/L Value
Power Supply	0.6-2.5V	0.6-2.5V
Power Consumption	12.5nW @ 120^0C, V_{DD} = 0.6V	1.05nW @ 120^0C, V_{DD} = 0.6V
Circuit area	0.0076mm^2	0.00013mm^2
Inaccuracy versus temperature	3^0C	6-7^0C
Inaccuracy versus V_{DD}	0.52^0C/V	0.47^0C/V
Sensitivity	1.41mV/^{0}C	0.354mV/^{0}C

Transient response	Stable at 17^0C	Sustained oscillations
Sink current	28nA @ 120^0C, V_{DD} = 0.6V	5nA @ 120^0C, V_{DD} = 0.6V
Transconductance	5.005 nA/V @ 25^0C, V_{DD} = 0.6V	0.815 nA/V @ 25^0C, V_{DD} = 0.6V
Transresistance	22.7 MΩ @ 25^0C, V_{DD} = 0.6V	416.6 MΩ @ 25^0C, V_{DD} = 0.6V

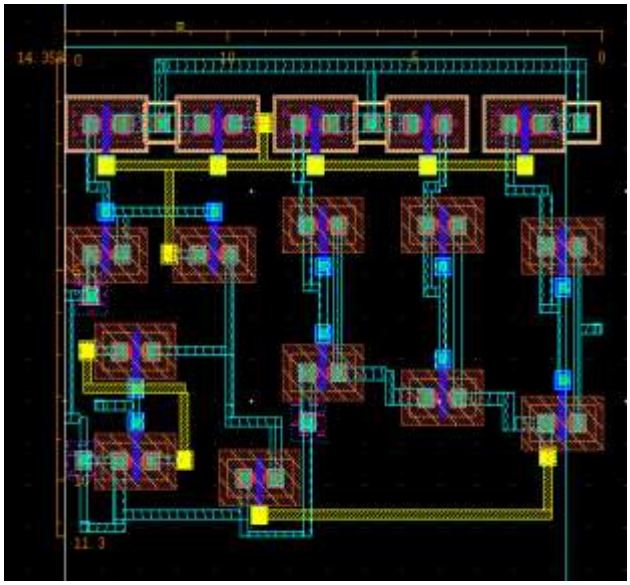


Fig 10. The layout of CMOS temperature sensor based aspect ratio

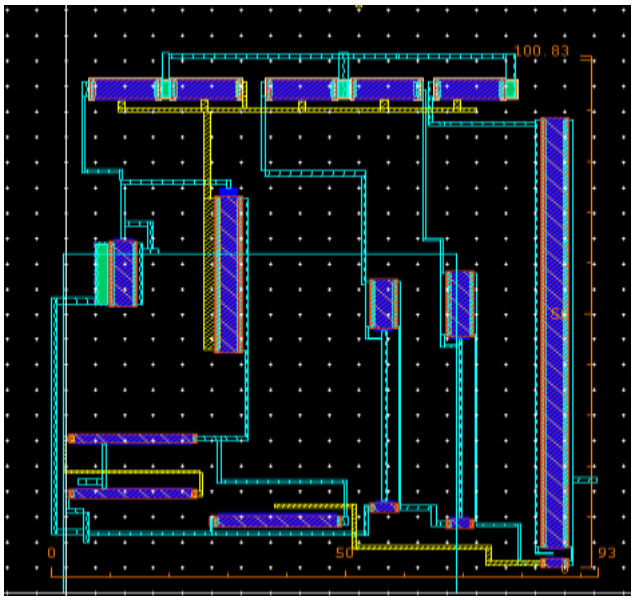


Fig 11. The layout of CMOS temperature sensor based on designed on minimum aspect ratio

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