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Review of a Digital Circuit Using Power Gating Techniques to Reduce Leakage Power

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ABSTRACT - Power dissipation is kept in consideration while implementing a digital circuit, On the other hand the process of scaling is used to analyze the output of that circuit. The process of scaling has its own limitations as the leakage current can flow out of the circuit due to scaling. The power dissipated from the circuit can be increased by making use of leakage current. The Power gating techniques are used to compensate the leakage current flowing through the digital circuit. This paper consist the nanometer technology being used to get different results. The process discussed above can be implemented and simulated by making use of TANNER suit using s-edit and T-SPICE at 130nm.

Key Words: Power gating circuits, Ground bounce noise, sleep methods, T- SPICE, H- SPICE.

1. Introduction:

The VLSI design system has increased the efficiency of our technological equipments by amending the various parameters such as reduction in power supply voltage by applying the process of scaling in fabrication process of CMOS design. These parameters has reduced the power dissipation but could not overcome the problems related to leakage current and circuit delay. To reduce the delay in circuit lower threshold voltage can be applied while at the same time leakage current can be reduced by CMOS logic. The use of a multi-threshold CMOS circuit, called a power gating structure widely use in all the portable devices. Power gating technique makes use of high threshold and low leakage devices such as sleep transistors, which isolates the idle blocks from the power supply and ground, or from the both. This technique uses higher Vt sleep transistors which disconnect VDD from a circuit block when the block is not switching.Power gatingis more beneficial than the clock gating. It increases the delay in time as the circuits modified with the power gating are to be safely entered and exited through power gated modes. Architecture experiences some power exchangesbetween leakagepowersused for designing and the power dissipation for entering and exiting the low power modes. The blocks can be shut down by the hardware or software. Power reduction operations can be can be optimized by the driver software. An alternate for this can be a power management controller. The power gating can be used to achieve leakage power reduction for long term by connecting an external power supply. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. Power gating is much more suitable for closing the blocks for a short span. CMOS switches are used to provide the power to the digital circuit and these CMOS switches are controlled by the power gating controllers.that provide power to the circuitry are controlled by power gating controllers..

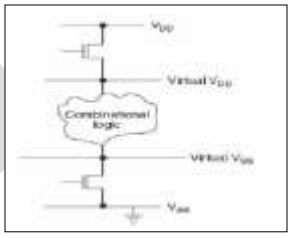

Fig 1. Power gated Circuit [1]

1.2 Ground Bounce

Due to shrinkness of a device at 130 nm and below, the signal integrity becomes a severe problem in VLSI circuits and is increasingly as per the reduction of size of circuit.The circuit noise is mainly caused due to inductive noise.The imposition of Moore's law results in faster clock speeds and larger number of I/O devices whereas it also results in higher amount of noise in power and ground planes.This inductive noise is sometimes referred to as the simultaneous switching noise because it is most pronounced when a large number of I/O drivers switch simultaneously.

2. Ground bounce reduction

In the general circuits using sleep transistors, some logic has separate power and ground pads, while other logic may share the power and ground pads. A certain length of PCB (Printed Circuit Board) transmission line connects each pad with the real power or ground. If the PCB has poorly layout, the transmission lines will contribute large parasitic capacitors and inductances, which can deteriorate the ground bounce effect when the sleep transistors are switched on. The parasitic capacitors, inductances depend largely on what types of the pads are and how the PCB layout is, however, many empirical data shows that these parasitic parameters can be quite considerable. The equivalent circuit of the logic using sleep transistors is shown in Figure 2. There are four parts of the equivalent circuit. Part I is the intrinsic capacitor, inductance and resistor of the power pad and the corresponding on-board transmission lines; Part II is the equivalent circuit of the functional logic; the sleep transistor is modeled as two resistors in Part III, where RST, ON <<RST, OFF. When the sleep transistor is turned on, it equals a small resistor which has negligibleeffect on the normal function of the circuit. When the sleep transistor is turned off, its resistor becomes hugeand cuts off the leakage path of the logic. Part IV is theintrinsic capacitor, inductance and resistor of the ground pad and the corresponding on-board transmission lines.

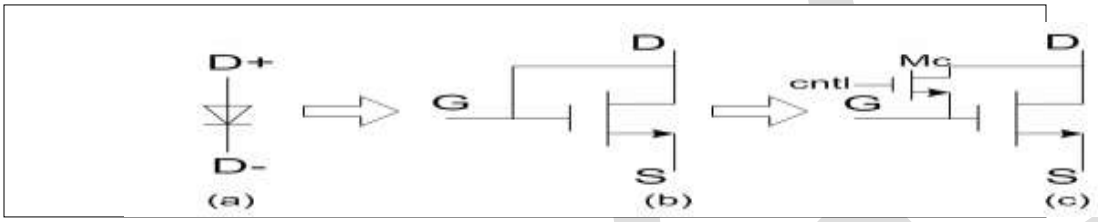

Fig 2. Ground bounces reduction logic [4]

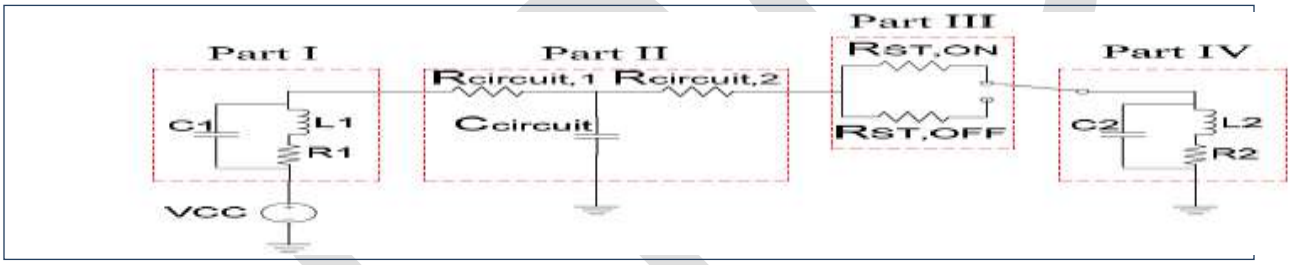

Fig 3. Equivalent circuit. [4]

4. Conclusion

We have done a review of scaling of power dissipation using power gating techniques. These power gating techniques are used to reduce the leakage current, circuit delay and ground bounce etc.

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