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Performance Evaluation of Adders using LP-HS Logic in CMOS Technologies

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ABSTRACT - This paper presents a modified approach for constant delay logic style named LP-HS logic. Constant delay logic style is examined against the LP-HS logic, by analysis through simulation. It is shown that the proposed LP-HS logic has low power, delay and power delay product over the existing constant delay logic style.Adders is one of the fundamental operations for any digital system. In this paper an 8 bit Ripple Carry Adder and 8 bit Carry Select Adder is analysed using both CD logic and LP-HS logic. The simulations were done using HSPICE tool in 45nm, 32nm, 22nm and 16nm CMOS technologies and performance parameters of power, delay and power delay product were compared. The adders using LP-HS logic is better in terms of power, delay and power delay product when compared to constant delay logic style.

Keywords— CMOS, MOSFET, VLSI, Power Consumption, Delay, Power delay product (PDP), Constant Delay Logic (CD logic)

INTRODUCTION

The need for high performance devices are increasing day by day. Rapid growth in VLSI technology enhancing all these features from generation to generation. The three most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are area, delay and power. Advances in CMOS technology have led to improvement in the performance in terms of area, power or delay. There always exists a trade-off between area, power and delay in a circuit. [2] The power delay product is a figure of merit for comparing logic circuit technologies or families. [1] Different types of logics are present in CMOS. The most common classification is the Static and Dynamic.[9] It is then further classified into other sub divisions.

One of the newly developed logic is the constant delay logic style.[7] This high performance energy efficient logic style has been used to implement complicated logic expressions. In this paper some modifications have been done for the constant delay logic style to reduce the power consumption and to improve the speed. The proposed technique is known as the LP-HS logic.

CONSTANT DELAY LOGIC STYLE

Designers of digital circuits often desire fastest performance. This means that the circuit needs high clock frequency. Due to the continuous demand of increase operating frequency, energy efficient logic style is always important in VLSI. One of the efficient logics which come under CMOS dynamic domino logic is the feedthrough logic (FTL). [3][4][5]Dynamic logic circuits are important as it provides better speed and has lesser transistor requirement when compared to static CMOS logic circuits. Feedthrough logic has low dynamic power consumption and lesser delay when compared to other dynamic logic styles.[11][13][14]

To mitigate the problems associated with the feedthrough logic new high performance logic known as constant delay (CD) logic style has been designed. It outperforms other logic styles with better energy efficiency. This high performance energy efficient logic style has been used to implement complicated logic expressions. It exhibits a unique characteristic where the output is pre-evaluated before the input from the preceding stage is ready.[7] Constant delay logic style which is used for high speed applications is shown in Fig 1.

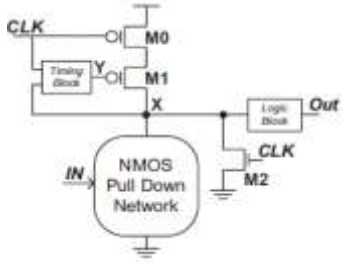


Fig 1: Constant Delay Logic Style [7]

CD logic consists of two extra blocks when compared to feedthrough logic. They are the timing block (TB) as well as the logic block (LB). Timing block consists of self reset technique and window adjustment technique. This enables robust logic operation with lower power consumption and higher speed. Logic block reduces the unwanted glitch and also makes cascading CD logic feasible. The unique characteristic of this logic is that the output is pre-evaluated before the inputs from the preceding stage got ready. An Nmos pull down network is placed where the inputs are given. Based on the logic which is given in the pull down network we will

get the corresponding output. A buffer circuit implemented using CD logic is shown below. The expanded diagram for timing block as well as logic block is also shown in the Fig 2

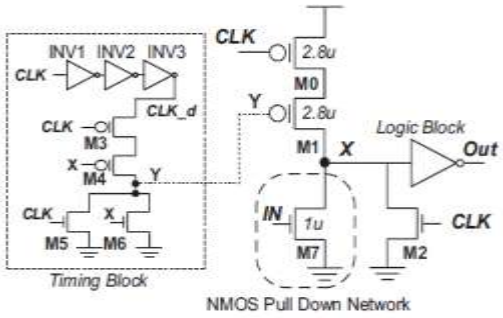


Fig 2: Buffer Using CD Logic [7]

The chain of inverters is acting as the local window technique and the NOR gate as a self reset circuit. Length of the inverter chain varies according to the circuit which we have to design. The prime aim of the inverter chain is to provide a delayed clock. The contention problem which is one of the disadvantages of the feedthrough logic is reduced with the help of this window adjustment. In the self reset circuit one of the input of the NOR gate is the intermediate output node X and the other one is the clock. The logic block is simply a static inverter as in the case of dynamic domino logic. Since the above circuit is for a buffer the NMOS pull down network consists of only one nMOS transistor.

The timing diagram for constant delay logic is shown in Fig 3.CD logic works under two modes of operation.

i. Predischarge mode (CLK=1)
ii. Evaluation mode (CLK=0)

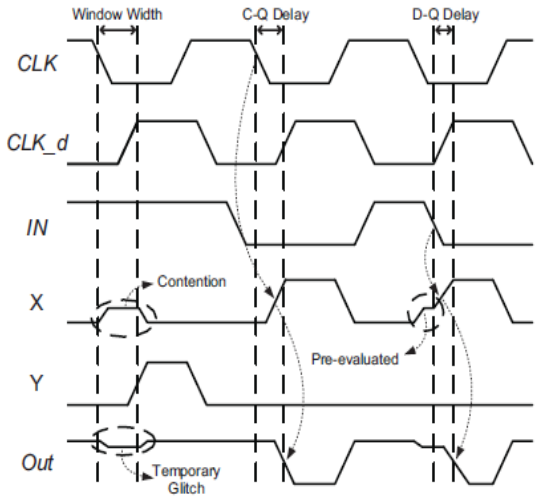


Fig 3: Timing Diagram of CD Logic [7]

Predischarge mode happens when CLK is high and evaluation mode occurs when CLK is low. During predischarge mode X and Out are predischarged and precharged to GND and VDD respectively. During evaluation mode three different conditions namely contention, C-Q delay and D-Q delay takes place in the CD logic. Contention mode happens when IN=1 for the entire evaluation period. During this time a direct path current flows from pMOS to PDN. X rises to nonzero voltage level and Out experiences a temporary glitch. C-Q delay (clock-out) occurs when IN goes to 0 before CLK transits to low. At this time X rises to logic 1 and Out is discharged to VDD and the delay is measured from CLK to Out. D-Q delay happens when IN goes to 0 after CLK transits to low. During this time X initially enters contention mode and later rises to logic 1 and the delay is measured from IN to Out.

If acknowledgement is there wishing thanks to the people who helped in work than it must come before the conclusion and must be same as other section like introduction and other sub section.

PROPOSED LP-HS LOGIC

The proposed LP-HS logic is derived from the existing constant delay logic. When compared to CD logic there are three major differences in the LP-HS logic. The window adjustment technique is eliminated in this logic. The evaluation transistor is altered

as pMOS transistor instead of nMOS. The third variation is the addition of the transistors M2 and M3 in parallel below the pull down network.

The proposed logic helps to reduce the power and delay which in turn reduces the power delay product. The circuit diagram for the proposed logic is shown in Fig 4

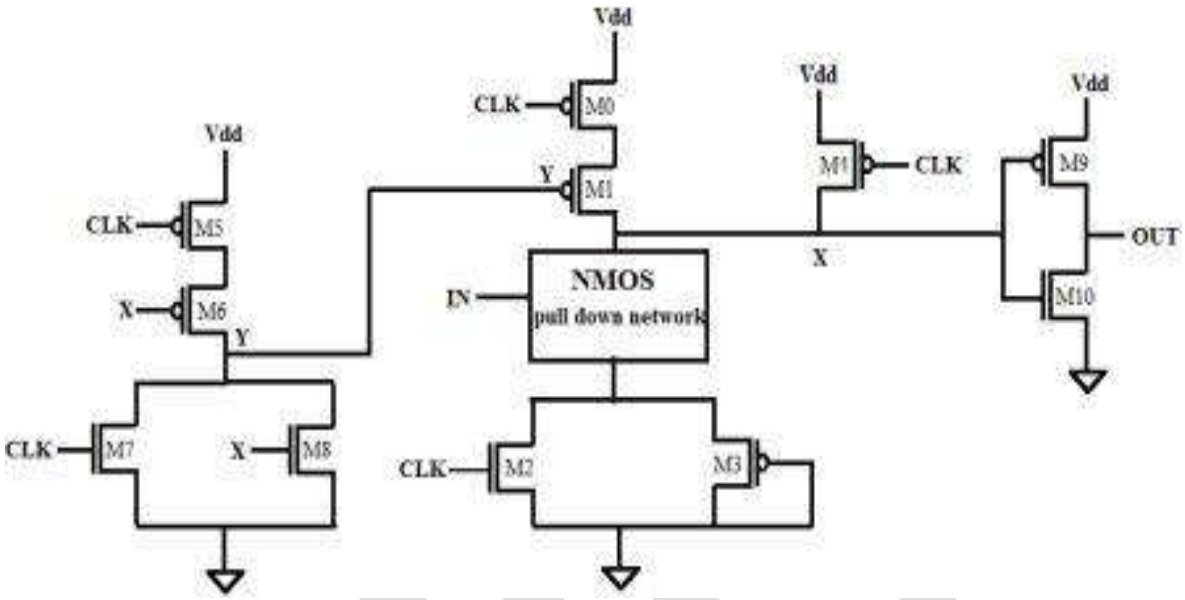


Fig 4: Proposed LP-HS Logic

Transistors M0 and M1 whose gates are driven by the CLK and the output of NOR gate are connected in series. This increases the resistance which in turn helps reducing the power. M4 is acting as an evaluation transistor. The NOR gate which is behaving as the self resetting logic is constituted by the transistors M5, M6, M7 and M8. M5, M6 and M7, M8 is driven by CLK and the output intermediate node X. IN values are given to the nMOS pull down network which is given according to the circuit which we have to design. Transistors M2 and M3 are connected in parallel and is placed down to the nMOS pull down network. These transistors help to reduce the power delay product. The gate of M2 is driven by the clock and M3 is at ground. Transistor M2 increases the dynamic resistance of the pull down network which successively helps to reduce the power consumption. Transistors M9 and M10 together figures the static inverter which is used to make the cascading logic more feasible.

The circuit works under two modes of operation.

i. Precharge mode (CLK=0)
ii. Evaluation mode (CLK=1)

Precharge mode occurs when clock is low and evaluation mode happens when clock is high. When clock is low, transistor M4 gets ON and provides a high value at node X which in turn provides a low value at the output node OUT. When clock is high the transistor M2 gets ON and the nMOS pull down network is evaluated and gives the output. During this time the transistor M0 whose gate is driven by the CLK is in OFF condition. Due to this the contention mode gets wiped out in the evaluation condition which in turn tends for the elimination of window adjustment technique in the proposed logic. One of the reasons for the power and delay reduction in the circuit is the elimination of the window adjustment technique. During the evaluation mode the pull down network and the transistor M2 gets ON which provides high dynamic resistance which further reduces the power. Transistor M3 is in always ON condition which offers an easy discharge of the value to the ground.

8 BIT RIPPLE CARRY ADDER

An 8 bit ripple carry adder is constructed by cascading FA blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry in of the next stage. An 8 bit ripple carry adder structure is shown in Fig 4 where x_0-x_7, y_0-y_7 represents the two set of inputs. C_0 represents carry input. The output sum and carry is shown as S_0-S_7 and C_7 respectively.

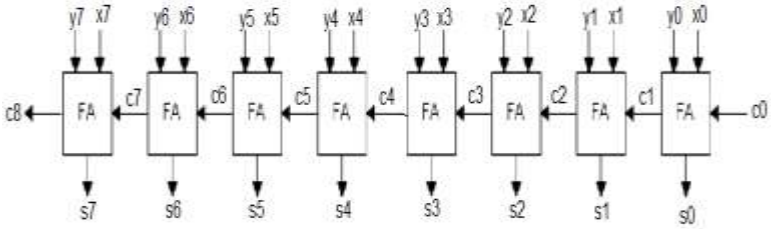


Fig 5: 8 Bit Ripple Carry Adder

SIMULATION RESULTS

Figure below describes the output waveforms of 8 bit ripple carry adder using both existing as well as proposed logic in different nanometer CMOS technologies. V(30,31,32,33,34,35,36,37), V(38,39,40,41,42,43,44,45) are the two input signals, V(46) refers the carry input. The output sum and carry are represented by V(55,56,57,58,59,60, 61,62) and V(54) respectively.

45nm CMOS TECHNOLOGY

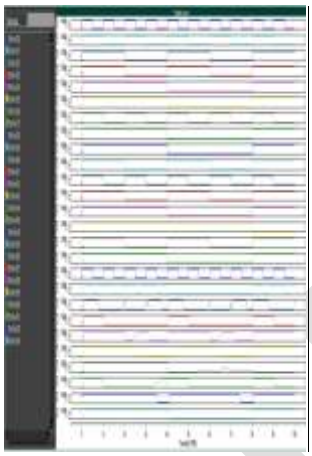


Fig 6: Output of Existing 8 bit RCA

Fig 7: Output of Proposed 8 bit RCA

32nm CMOS TECHNOLOGY

Fig 8: Output of Existing 8bit RCA

Fig 9: Output of Proposed 8 bit RCA

22nm CMOS TECHNOLOGY

Fig10: Output of Existing

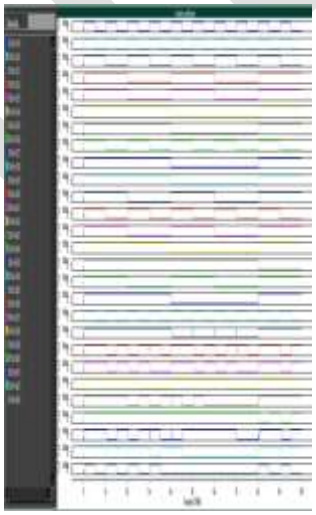


Fig11:Output of Proposed

16nm CMOS TECHNOLOGY

Fig 12:Output of Existing

Fig 13:Output of Proposed

8 bit RCA ***8 bit RCA*** ***8bit RCA*** ***8 bit RCA***

8 BIT CARRY SELECT ADDER

The concept of carry select adder (CSA) is to compute alternative results in parallel and subsequently selecting the correct result with a single or multiple stage hierarchical techniques. In order to enhance its speed performance, the carry select adder increases its area requirements. In carry select adders both sum and carry bits are calculated for the two alternatives: inputs carry '0' and '1'. Once the carry in is delivered, the correct computation is chosen (using a MUX) to produce the desired output. Therefore instead of waiting for the carry in to calculate the sum, the sum is correctly found as soon as the carry in gets there. The time taken to compute the sum is then avoided which results in good improvement in speed. An 8 bit carry select adder structure is shown in Fig 7 x_0-x_7, y0-y_7 represents the two set of inputs. C_0 represents carry input. The output sum and carry is shown as S_0-S_7 and C_7 respectively.

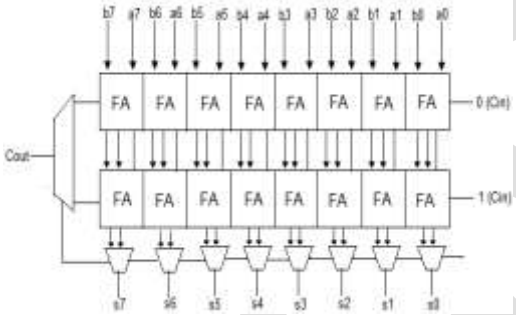


Fig 14: 8 Bit Carry Select Adder

SIMULATION RESULTS

Figure below describes the output waveforms of 8 bit carry select adder using both existing logic as well as proposed logic in different nanometer technologies. V(2,3,4,5,6,7,8,9), V(10,11,12,13,14,15,16,17) are the two input signals, V(20) refers the carry input. The output sum and carry are represented by V(21,22,23,24,25,26,27,28) and V(39) respectively.

45nm CMOS TECHNOLOGY

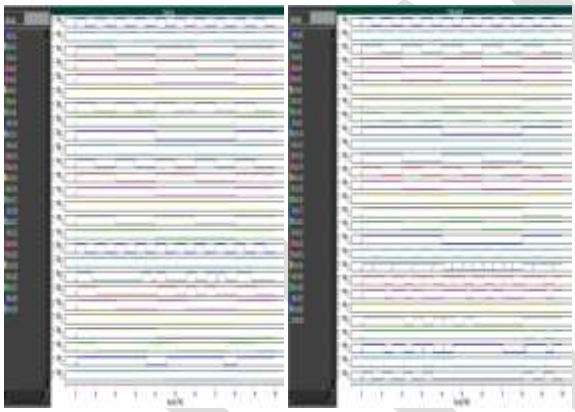
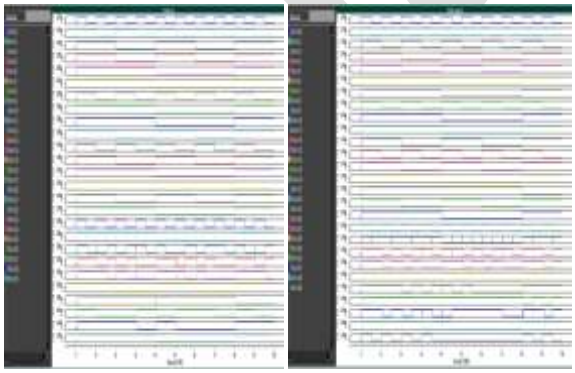


Fig15: Output of Existing 8 bit CSA ***Fig16: Output of Proposed 8 bit CSA***

32nm CMOS TECHNOLOGY

Fig17: Output of Existing 8bit CSA ***Fig18: Output of Proposed 8 bit CSA***

22nm CMOS TECHNOLOGY



16nm CMOS TECHNOLOGY

Fig19: Output of Existing 8 bit CSA *Fig20: Output of Proposed 8 bit CSA* *Fig21: Output of Existing 8bit CSA* *Fig22: Output of Proposed 8 bit CSA*

PERFORMANCE ANALYSIS

Here the performance analysis like power, delay and power delay product of 8 bit RCA and 8 bit CSA using CD logic as well as LP-HS logic have been carried out and there results were compared and is shown in the table below.

Table 1: Power, Delay and PDP analysis of 8 bit RCA in different nanometer technologies

TECHNOLOGY	CD LOGIC			LP – HS LOGIC		
	Power (µw)	Delay (ps)	PDP (fJ)	Power (µw)	Delay (ps)	PDP (fJ)
45nm	77.10	8.35	0.64	13.46	8.30	0.11
32nm	58.15	38.64	2.24	8.39	35.35	0.30
22nm	88.04	11.85	1.04	6.92	21.21	0.15
16nm	8.52	9.30	0.08	2.41	17.86	0.04

Table 2: Power, Delay and PDP analysis of 8 bit CSA in different nanometer technologies

TECHNOLOGY	CD LOGIC			LP – HS LOGIC		
	Power (µw)	Delay (ps)	PDP (fJ)	Power (µw)	Delay (ps)	PDP (fJ)
45nm	164.30	38.96	6.40	44.92	21.17	0.95
32nm	125.50	73.69	9.24	29.91	67.61	2.02
22nm	207.60	27.46	5.70	21.77	40.65	0.88
16nm	18.86	42.11	0.79	5.61	61.52	0.35

CONCLUSION

The concept of constant delay logic is modified and a new logic has been developed known as the LP-HS logic. Adders are designed using both existing as well as proposed logic. It is simulated with 45nm, 32nm, 22nm and 16nm CMOS technologies and the performance parameters power, delay, power delay product were compared. The simulations for 45nm, 32nm and 22nm CMOS technologies were carried out at 0.9 V, while 16nm CMOS technology was simulated at 0.6V. The operating frequency for all the technologies was kept at 1GHz.

From the results it is found that the power delay product has been improved by 82.81% for 8 bit RCA and 85.15% for 8 bit CSA using the proposed logic in 45nm CMOS technology. A betterment of 86.60% has been found for 8 bit RCA and 78.13% for 8 bit CSA using the proposed logic for 32nm CMOS technology. Similarly an improvement of 85.57% for 8 bit RCA and 84.56% for 8 bit CSA were found using the proposed logic in 22nm CMOS technology. Finally an improvement of 50% and 55.69% have been found for 8 bit RCA and 8 bit CSA in 22nm CMOS technology.

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