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Performance Evaluation of Guarded Static CMOS Logic based Arithmetic and Logic Unit Design

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ABSTRACT – Real World applications tend to utilize the improved low power processes to reduce power dissipation and to improve the device efficiency. With regards to this unique aspect, optimization techniques help in reducing down the parameters like power and area which are of a major concern. The commonly found arithmetic and logic unit in every processor is likely to consume more power for its internal operations. This power consumed can be reduced using the low power optimization techniques. With reference to the above issue, in this paper an efficient Arithmetic and Logic unit is designed with a modified static CMOS logic design. This modified logic is found to be more efficient than the existing logic in terms of many parameters like average power and power delay product. This way the modified architecture of arithmetic and logic unit in different CMOS technologies performs the processing with high speed.

Keywords— Low power, modified static CMOS logic, power delay product, arithmetic and logic unit

I.INTRODUCTION

Very Large Scale Integrated (VLSI) circuit technology is a rapidly growing technology for a wide range of innovative devices and systems that have changed the world today. The tremendous growth in laptop and portable systems and the cellular networks have intensified the research efforts in low power electronics [1]. High power systems often may lead to several circuit damages. Low power leads to smaller power supplies and less expensive batteries. Low-power design is not only needed for portable applications but also to reduce the power of high performance systems. With large integration density and improved speed of operation, systems with high frequencies are emerging.

The arithmetic logic unit is one of the main components inside a microprocessor. It is responsible for performing arithmetic and logic operations such as addition, subtraction, increment, and decrement, logical AND, logical OR, logical XOR and logical XNOR [2]. They use fast dynamic logic circuits and have carefully optimized structures [3]. Its power consumption accounts for a significant portion of total power consumption of data path. Arithmetic and Logic Units (ALU) also contributes to one of the highest power-density locations on the processor as it is clocked at the highest speed and is kept busy most of the time resulting in thermal hotspots and sharp temperature gradients within the execution core. Therefore, this strongly motivates energy-efficient ALU designs that satisfy the high-performance requirements, while reducing peak and average power dissipation. ALU is a combinational circuit that performs arithmetic and logical micro-operations on a pair of n bit operands [4]. The power consumption in digital circuits, which mostly use complementary metal-oxide semiconductor (CMOS) devices, is proportional to the square of the power supply voltage; therefore, voltage scaling is one of the important methods used to reduce power consumption. To achieve a high transistor drive current and thereby improve the circuit performance, the transistor threshold voltage must be scaled down in proportion to the supply voltage [5].

II.EXISTING ALU DESIGN

The existing method includes a simple Arithmetic and Logic Unit design with different arithmetic and logic operations [10]. The existing basic design consists of a conventional type of arithmetic and logic circuits that perform various arithmetic and logic operations required shown in Fig 2.1.These conventional circuits are designed in CMOS logic. When the architecture is simulated, it is found to consume more power and it is the main disadvantage of the existing systems.

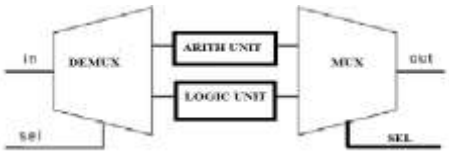

Fig 2.1 Basic Concept of ALU design

The existing feed through Logic, given in Fig 2.2, works in two phases, Reset phase and Evaluation phase [11], [12]. It can be shown, when clock is 'HIGH', the output node is pulled to zero value because transistor Tr is 'ON' and transistor TP is 'OFF'. When clock goes 'LOW', reset transistor Tris turned 'OFF' and Tpbecomes 'ON' resulting in charging or discharging of output node with respect to input. Reset Transistor Tralways provides 0->1 transition, initially in evaluation phase, therefore outperforms the dynamic CMOS in cascading structure. When dynamic CMOS is cascaded, produced result may be false due to 1-> 0 transitions in evaluation phase.

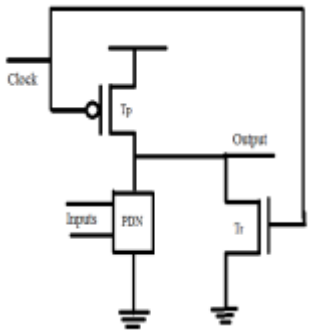

Fig 2.2 Existing Feed through Logic

III.PROPOSED ALU DESIGN

The proposed system uses a guarded static logic principle which is explained below. The Fig 3.1 below shows a simple low power technique. This simple modified technique is designed with two control inputs. It works similar to the existing static CMOS logic in which during the high phase of clock, the output node does not give the exact output. When clock becomes low the output node conditionally evaluates to either logic high or low, depending on the inputs to pull up and pull down networks present in the circuit.

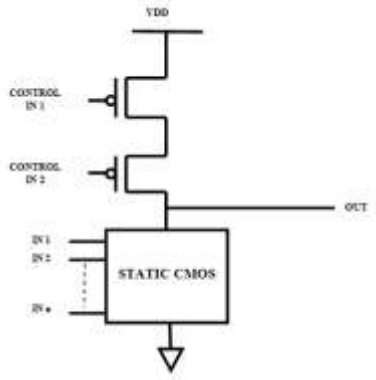

Fig 3.1 Proposed Technique (Guarded static CMOS logic)

The proposed system consists of a modified Arithmetic and Logic Unit, which includes a modified architecture with the proposed Guarded Static CMOS logic logic (GSCL). Hence an additional loss in power consumption of the circuit is further observed. The modified arithmetic and logic unit block with the control unit is shown in Fig 3.2 below. According to the block diagram below, each block is fed with two control signals. One of the control signals chooses whether the operation to be executed is arithmetic block or logic block. The second control signal chooses which particular block needs to be executed. Hence the choice is made by the user in providing the arithmetic and logic unit with the necessary control input.

Fig 3.2 depicts the main architecture of the paper. There are different blocks that are interlinked to form a complete architecture. For this control signal to be activated inside a particular block, each block is modified with low power techniques to reduce the power consumption that gets wasted because of the execution of all other processing blocks. Using these techniques, only a single arithmetic or logic block is activated and its output is achieved in accordance with the control signal provided. The low power

technique for this requirement used is discussed below. This way the design is made simple and the processing is done in a continuous manner and used in bigger circuits to compensate for high power dissipation.

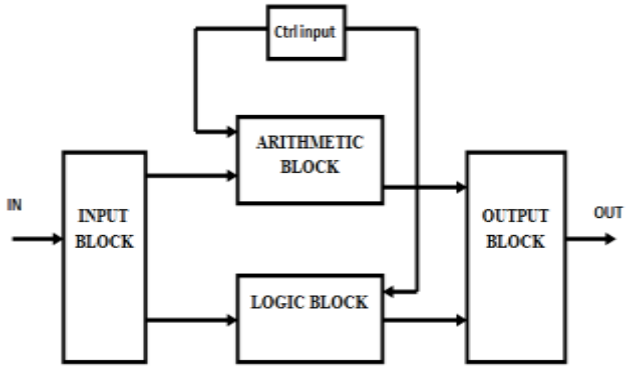

Fig 3.2 Modified Architecture of Arithmetic and Logic unit

3.1 DESCRIPTION OF ARCHITECTURE

3.1.1 Input Block:

Input block consists of two general purpose registers. These registers provide the necessary inputs to the arithmetic and logic unit blocks. These blocks functions various arithmetic and logic operations.

3.1.2 ALU Block:

This arithmetic block consists of four bit adder, subtractor, right and left shifter, comparator, encryption and decryption circuit and multiplier. The logic block consists of four bit AND, OR, NOT, NAND, NOR, XOR and XNOR gates. This architecture is modified in such a way that from the control unit above, instructions are fed to choose a particular operation to be performed and only the execution of that particular operation reaches the output port of the processor. Hence this saves time in turn the power consumption gets reduced to a greater extent than the existing system.

3.1.3 Output Block:

The output block consists of a simple OR gate whose inputs are the outputs from the 8 units of ALU block. Since only one block outputs a true value, the necessity of an OR gate gets fulfilled here. This is how a simple output block is designed in this paper.

IV. TRANSIENT ANALYSIS

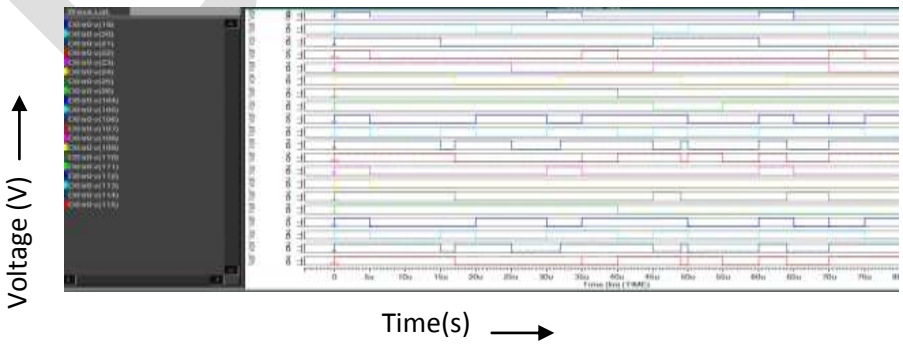

Fig 4.1Transient analysis of existing arithmetic and logic unit

Fig 4.1 shows the output waveform of existing 4-bit arithmetic and logic unit in which v(19)-v(26) represents the ALU input v(104)-v(107) represents the arithmetic unit output, v(108)-v(111) represents the logic unit output, v(112)-v(115) represents the ALU output.

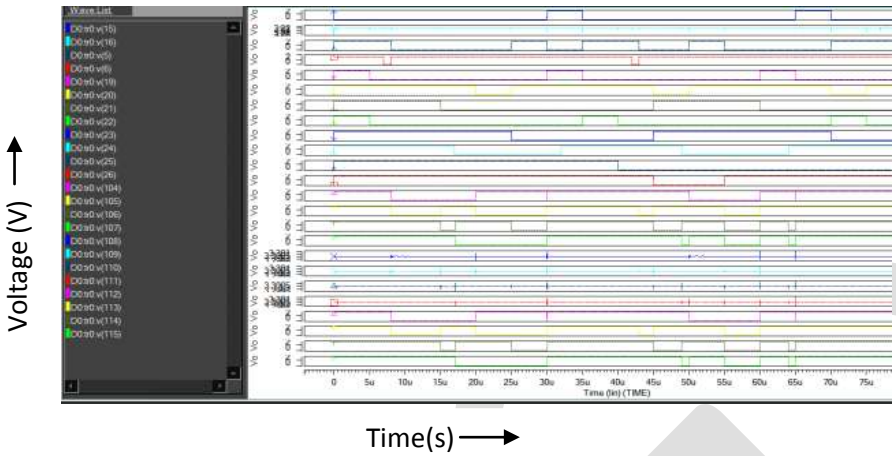

Fig.4.2 Transient analysis of proposed Arithmetic and logic unit

Fig.4.2 shows the output waveform of proposed Arithmetic and logic unit in which v(15),v(16),v(5),v(6) represents control inputs v(19)-v(26) represents the ALU input v(104)-v(107) represents the arithmetic unit output, v(108)-v(111) represents the logic unit output, v(112)-v(115) represents the ALU output.

V. POWER ANALYSIS

Table 5.1 Power Analysis of Existing System and Proposed System

DEVICE:MOSFET TECHNOLOGY:130nm OPERATING FREQUENCY:1GHz						
DESIGN	**EXISTING**			**PROPOSED**		
ALU DESIGN	**Avgpwr (µw)**	**Delay (µs)**	**PDP (pJ)**	**Avgpwr (µw)**	**Delay (µs)**	**PDP (pJ)**
	126.6	2.002	253.45	101.19	0.009	0.910

Table 5.2 Power Analysis of Existing System and Proposed System

DEVICE:MOSFET TECHNOLOGY:32nm OPERATING FREQUENCY:1GHz						
DESIGN	**EXISTING**			**PROPOSED**		
	Avgpwr	**Delay**	**PDP**	**Avgpwr**	**Delay**	**PDP**

ALU DESIGN	(µw)	(µs)	(pJ)	(µw)	(µs)	(pJ)
	3967	2.026	8037.1	11.94	0.009	0.107

Table 5.3 Power Analysis of Existing System and Proposed System

DEVICE:MOSFET TECHNOLOGY:16nm OPERATING FREQUENCY:1GHz						
DESIGN	**EXISTING**			**PROPOSED**		
ALU DESIGN	**Avgpwr (µw)**	**Delay (µs)**	**PDP (pJ)**	**Avgpwr (µw)**	**Delay (µs)**	**PDP (pJ)**
	513.8	2.026	1040.9	20.86	0.009	0.18

The above Tables 5.1, 5.2 & 5.3 shows the performance analysis report for existing and modified arithmetic and logic circuit with the Guarded static CMOS logic technique in three different CMOS nanometer technologies

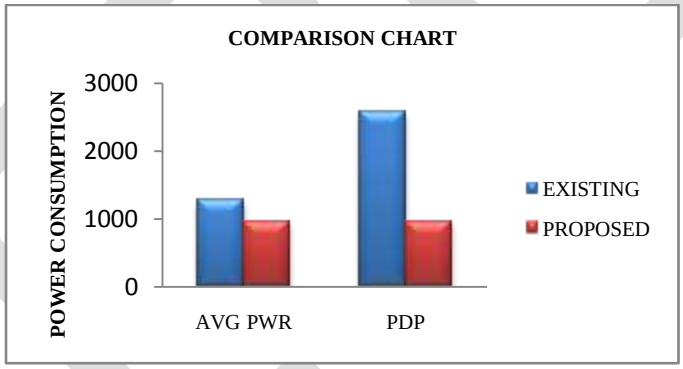

Fig5.1 Power consumption comparison of existing and proposed system

The above chart in Fig 5.1 shows the comparative performance of ALU with operating voltage of 3.3V using HSPICE in 130nm CMOS technology. The analysis clearly shows that the arithmetic and logic unit in the existing system consumes 126.6 µW of power and the proposed system consumes a considerable less amount of 101.19µW of power. When the controlled feed through logic is used in the ALU circuit, the power consumption experiences a drastic reduction increasing the speed of the device.

CONCLUSION

Thus the power consumption is greatly reduced in the modified design using the Guarded static CMOS logic and it is found to be more efficient. With the conventional type of arithmetic and logic unit that executes all the operations at the same time, the power dissipation gets uncontrolled. Hence to discover an alternative, this static CMOS logic was taken as a base and a proposed Guarded Static CMOS logic was introduced. The performance analysis clearly shows that the arithmetic and logic unit designed using Guarded Static CMOS logic shows appropriate dimensions of various parameters helping to obtain a near optimum arithmetic and logic circuit. Hence the power consumption of the modified ALU design is further reduced. The proposed Arithmetic and Logic Unit design can be used in high end real time applications like ARM processors and also in various other low power applications.

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