International Journal of Engineering Research and General Science Volume 2, Issue 6, October-November, 2014
ISSN 2091-2730

Optimal Low Switching Frequency Pulsewidth Modulation of Fifteen-Level Hybrid Inverter

Vasanth V[1], Prabu M[2]

[1] PG scholar Department of EEE, Nandha Engineering College, Erode, India

[2] Associate professor Department of EEE, Nandha Engineering College, Erode, India.

Corresponding author: vasanthpaul23.v@gmail.com, prabunec2013@gmail.com

Abstract—The object of this paper is to operate a fifteen-level Hybrid inverter of an induction motor drive at an average device switching frequency limited to rated fundamental frequency by using Synchronous optimal pulse width modulation(SOP) technique. To reduce the number of separate dc sources, a three-level transistor clamped inverter was used as a cell in the fifteen-level hybrid inverter. Using SOP technique, optimal fifteen-level waveforms were obtained by offline optimization assuming steady-state operation of the induction machine. The switching angles for each semiconductor switch are then obtained from optimal fifteen-level waveforms based on the criteria to minimize the switching frequency as well as unbalance in dc-link capacitor voltages. Simulation results obtained from the 1.5-kW induction motor drive show THD <5% for stator currents. The results indicate that SOP technique reduces the switching frequency of operation without compromising on THD.

Keywords— Transistor clamped, H-bridge, medium-voltage ac drives, synchronous optimal pulse width (SOP) modulation.

I INTRODUCTION

Multilevel inverters are now well-established and standard solution for medium and high-voltage, high power applications and power-quality demanding solutions. The advantages of multilevel inverters over two-level inverters are higher voltage operating capability with medium voltage semiconductor devices, improved output voltages with less harmonic distortion, lower common-mode voltages, less *dv /dt* stress, near sinusoidal input currents, smaller input and output filters, increased efficiency due to possibility of low switching operation, reduced electromagnetic interference problems and possible fault-tolerant operation [1]–[9]. In addition, the torque ripple also reduces as number of levels increases in case of multilevel inverter fed ac drives. In high-power applications, the switching losses contribute to major portion of total device losses andthus low switching frequency operation is necessary to achieve higher efficiency.However, minimizing switching frequency increases the harmonic distortion. Therefore, the challenge is to minimize the harmonic distortion while reducing the switching frequency. Presently, the most popular topologies are diode-clamped or neutral-point-clamped (NPC), capacitor-clamped or flying capacitor (FC) and cascaded H-Bridge (CHB) [3]. The CHBtopologies are preferred for higher-level inverters due to requirementof least number of components and ease of controlcompared to other topologies. In addition, modularized circuitlayout and packaging is also possible with CHB topology becauseeach level has similar structure [10]. However, one major drawback of this topology is requirement of multiple numbers of dc-sources, which is not feasible in many applications. One ofthe method for reducing the number of dc sources is to replace H-Bridge cell with NPC or FC inverters [11]. However, an important issue with the topologies having NPC or FC invertersis voltage unbalance of dc-link capacitors that further addsto harmonic distortion of output voltage waveforms. An auxiliary capacitor-based balancing approach has been proposed to equalize the dc-link capacitor voltages for NPC five-level inverter [12].Several low switching frequency modulation techniques have been proposed for high-power applications. A new modulation method for modular multilevel inverter operating at fundamental switching frequency while successfully eliminating fifth harmonic was proposed in [13]. A novel switching sequence design for the space-vector modulation (SVM) of high-power multilevel inverters optimized for the improvement of harmonic spectrum and the minimization of device switching frequency was proposed in [14]. A new control method for seven-level cascaded inverter operating at fundamental switching frequencywas proposed by Zhong Du *et al.* [15].Model predictive currentcontrol algorithm has been demonstrated for CHB nine-levelinverter with switching frequency between 425 to 500 Hz [16].Also, an adaptive duty-cycle modulation algorithm that reducesthe switching frequency by using the slope of the voltage reference to adapt the modulation period was proposed by Kouro*et al.* [17]. By using this method, the switching frequency of operation has been maintained between 285 to 785 Hz for fifteen level asymmetric CHB inverter. The selective harmonic elimination (SHE) method is one of the low-switching frequency control technique which eliminates($n - 1$) lower order harmonic components, n being the number of switching angles. Generalized SHE technique in Fourier domain for two-level single phase and three phase inverters has been proposed by patel *et al.*

[18], [19]. Programmed PWM technique for minimizing the harmonics has been reported. [20], [21]. A new method for SHE based on six-step symmetry[22] and by use of Walsh functions to obtain Fourier spectral equations has been reported [23], [24]. A new solution to convert the transcendental equations into polynomial equations for SHE has been proposed [25]. The general problem formulationand selected solutions for both unipolar and bipolar switching patterns to eliminate the fifth and seventh harmonics are presented by Wells *et al.* [26]. A novel method to achieve fasttransient response and efficient harmonic (disturbance) filteringhas been achieved by using signal processing methods [27]. A minimization method to derive multiple sets of solutions forthe bipolar SHE PWM method for both single-phase and three phase inverters has been presented in [28]. A real-time method by using modified triangle carrier has been proposed insteadof conventional offline solution of switching angles [29].In this method, initial guess is not required as well as switching frequency is not restricted to integer multiple of fundamental frequency [30]. SHE is also extended for multilevel inverters.A unified approach to solving the harmonic elimination equationsin multilevel inverter to obtain the switching angles inthe lower range of modulation indices has been reported [31].A Bee algorithm for SHE has been reported by Kavousi et al for cascaded multilevel inverter [32]. In steady-state operating conditions, SOP method for controlling five-level inverters [33], [34] and dual three-level inverters [35], [36] with maximum switching frequency of 200 Hz have been demonstrated. In case of high performance drives which are subjected to frequent transient conditions, using traditional closed-loop control techniqueswith SOP technique intervenes with optimal switching patterns and hence, a real-time optimization is required. Thus, initially optimal stator current trajectory tracking method has been proposed [37], [38]. Then, trajectory of an optimal statorflux vector which is independent of machine parameters or load conditions has been suggested as tracking agent [39]–[42].Nonetheless, the application of SOP has not been reported for multilevel inverters with more than five-levels. Therefore, the objective of the present study is to demonstrate SOP technique for operating nine-level cascade inverter of induction motor drive at an average device switching frequency limited to rated fundamental frequency (50 Hz) in open loop (v,f) control mode. It should be pointed out that proposed SOP technique can be used for any fifteen-level inverter topology by modifying the method of assigning switching angles for each power semiconductor switch based on optimal fifteen-level waveforms.

IIHYBRID MULTI LEVEL INVERTER TOPOLOGY

The hybrid multilevel inverter is a series connection of cascade half bridge cell and H-bridge inverter. In recent years multilevel inverters have been paying attention on and preferred as high power and high voltage ones [5]. Use of multilevel inverters is becoming popular for high power applications especially in the distributed generation where a number of batteries, fuel cells, solar cell, and micro-turbines can be connected through a multilevel inverter to feed a load or the ac grid without voltage balancing problems. Another major advantage of hybrid multilevel inverters is that their switching frequency is lower than a traditional low-level inverter, which leads to reduced switching losses. The topologies for high power multilevel inverters are classified into three types as shown in Fig 1. The transistor clamped inverter, the flying capacitor inverter and the H-bridge inverter.

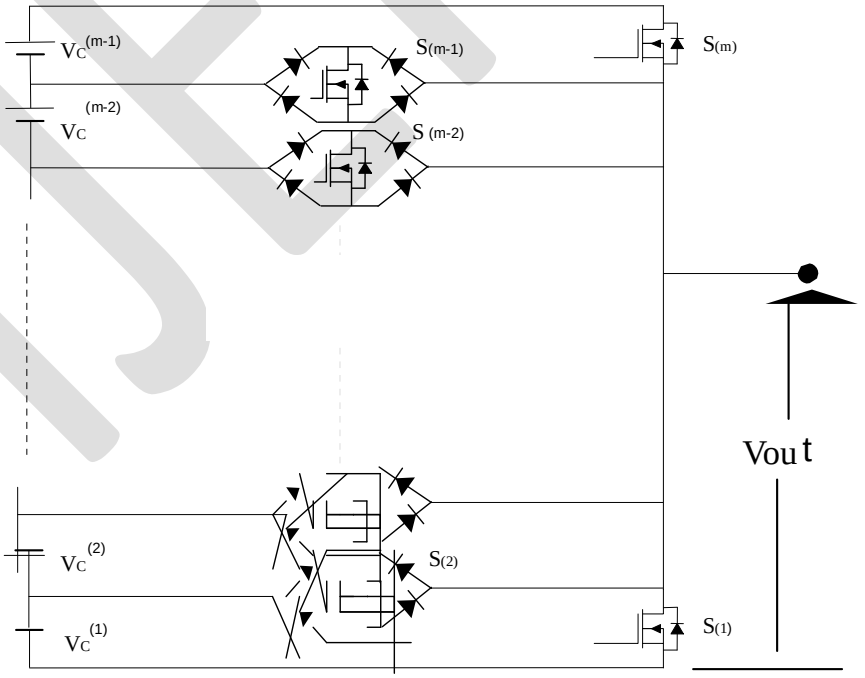

Fig 1: Multilevel Inverter Topologies

Among these inverters, the cascaded inverter has the advantages that the DC-link voltage is balanced, circuit layout flexibility, Cascaded multilevel inverterarchitecture has the ability to tolerate a fault for several cycles but if the fault typeand location can be detected and identified, compared with the diode-clamped and flying capacitor inverters it requires the least number of components to achieve the same number of voltage levels, switching patterns and the modulationindex of other active cells can be adjusted to maintain the operation under abalanced load condition.

Multilevel PWM and harmoniceradication are techniques that can be used in cascade multilevel inverters in orderto achieve voltage waveforms with low total harmonic distortion (THD) withminimum switching losses and low filtering necessities. Using a multilevel layout, an effectual high switching frequency can beachieved in the output voltagewaveform with each of the H-bridge modules havinga relatively low switching frequency as shown in Fig 2. This approach will facilitateincreased converter efficiency. Tumbling the filtering requirements would help toreduce the cost and improve the reliability and dynamic performance of the wholesystem.

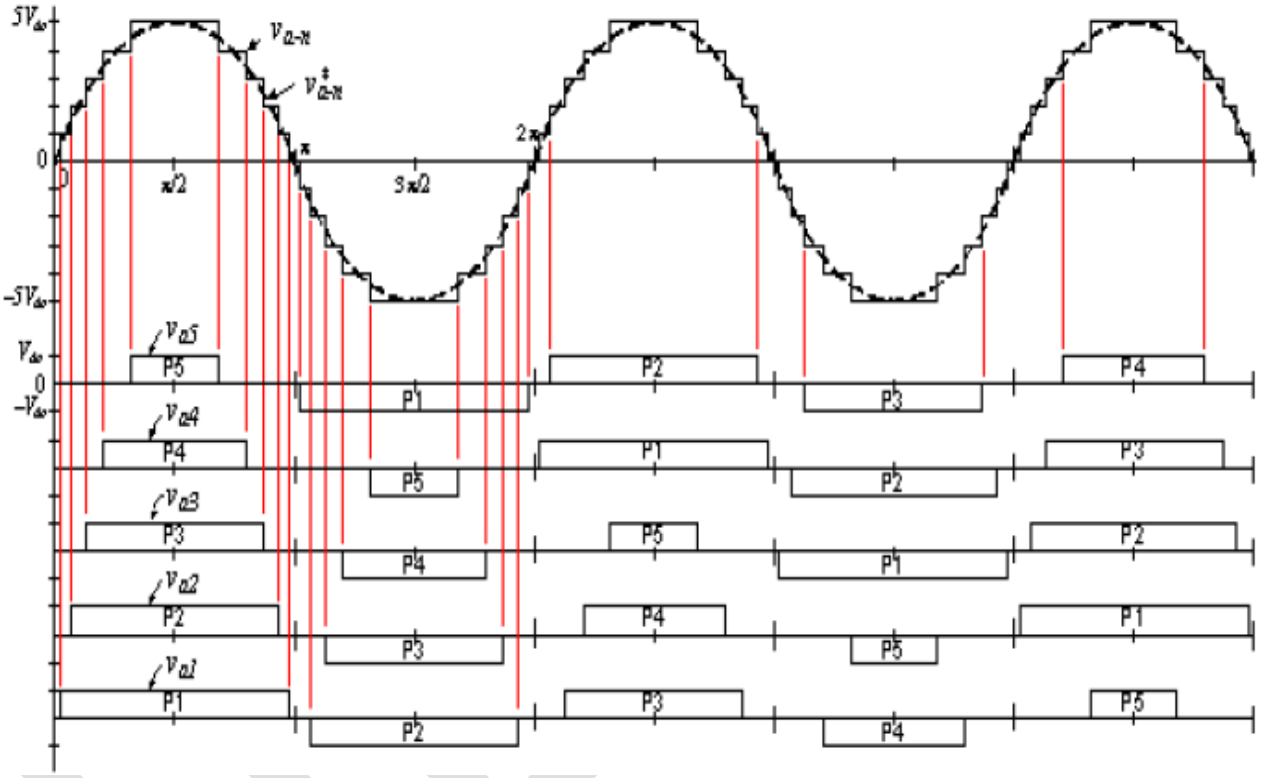

Fig2:Low loss low switching frequency multilevel inverter waveforms.

III. SYNCHRONOUS OPTIMAL PULSEWIDTHMODULATION (SOP)

SOP generates optimal switching pulse patterns of semiconductor devices in a multilevel inverter [43]. Synchronized PWM is used in low-switching frequency applications where carrier signal at frequency (f_s) and sinusoidal control signal at frequency (f_1) are synchronized with each other, i.e., f_s/f_1 is an integer in order to eliminate sub harmonic frequencies which are undesirable in many applications. Synchronized PWM results in lower number of switching instants per fundamental period and even a little variation in these switching angle values will have considerable influence on the harmonic distortion of output voltage [44]. Optimization methods are suggested to predetermine switching angles offline to reduce harmonic distortion [45]. The precalculated switching angles are stored and retrieved during real-time operation.

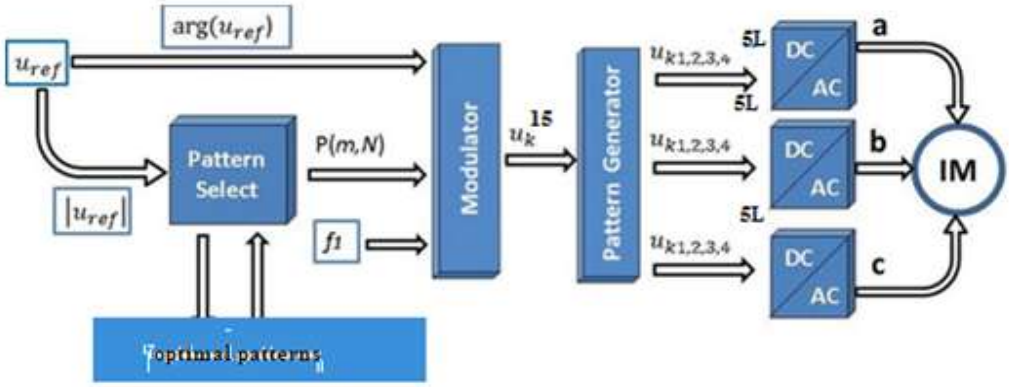

Figure 3.1 Signal Flow Graph of Fifteen level Inverter

3.1 Optimization Method

The goal of optimization is to generate optimal switching patterns for each steady state operating point (*m*, *N*) in order to minimize DF. The flowchart of optimization algorithm is shown in Fig. 5. The constraints of optimization are as follows [33]:

1) Sufficient gap (10 μs) between consecutive switching angles to allow for minimum ON times and OFF times of the power semiconductor devices;

2) In order to maintain current modulation index value, it is mandatory to satisfy the relation (9);

3) Continuity of switching angles for a given pulse number over its associated modulation index range in order to avoid transients in machine currents.

In the beginning, all the possible structures for N = 4 to 13are obtained in the form of switching transitions *s (i)*. For each pulse number *N*, modulation index range is determined and then for each operating point (*m*, *N*), MATLAB function "random" is used to generate the initial values of switching angles for further optimization while satisfying the relation (9).

We are performed computer-aided simulations to prove availability of the proposed multilevel inverter. The simulations are implemented using Matlab and it was considered to a pure resistive load. The conventional method simulation output has been obtained by using the carriers. In this proposed method the output has been obtained by using the Matlab/Simulink.

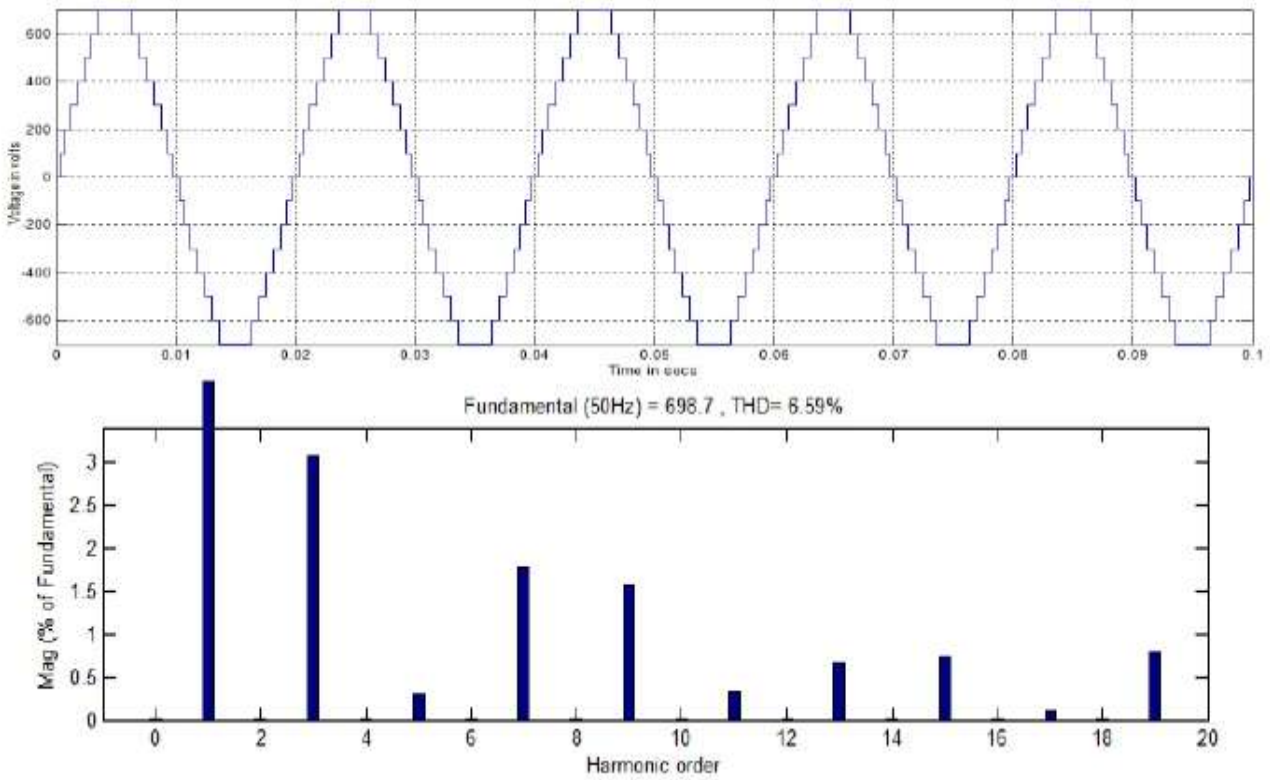

Figure 3.2 Model Simulation Results

IV SIMULATION RESULTS

Simulation of a 15-level multilevel inverter uses four variable dc sources to minimize the harmonics. Four variable dc sources are V1=81.5, V2=81.5, V3=81.5 & V4=163. This simulation achieves a speedup of 500x and the execution time range is 20 mille seconds. The output voltage of 15 levels multilevel inverter as shown in Fig 5.The solution of this approach is 4.81% of THD by using genetic algorithm as shown in Fig.6.

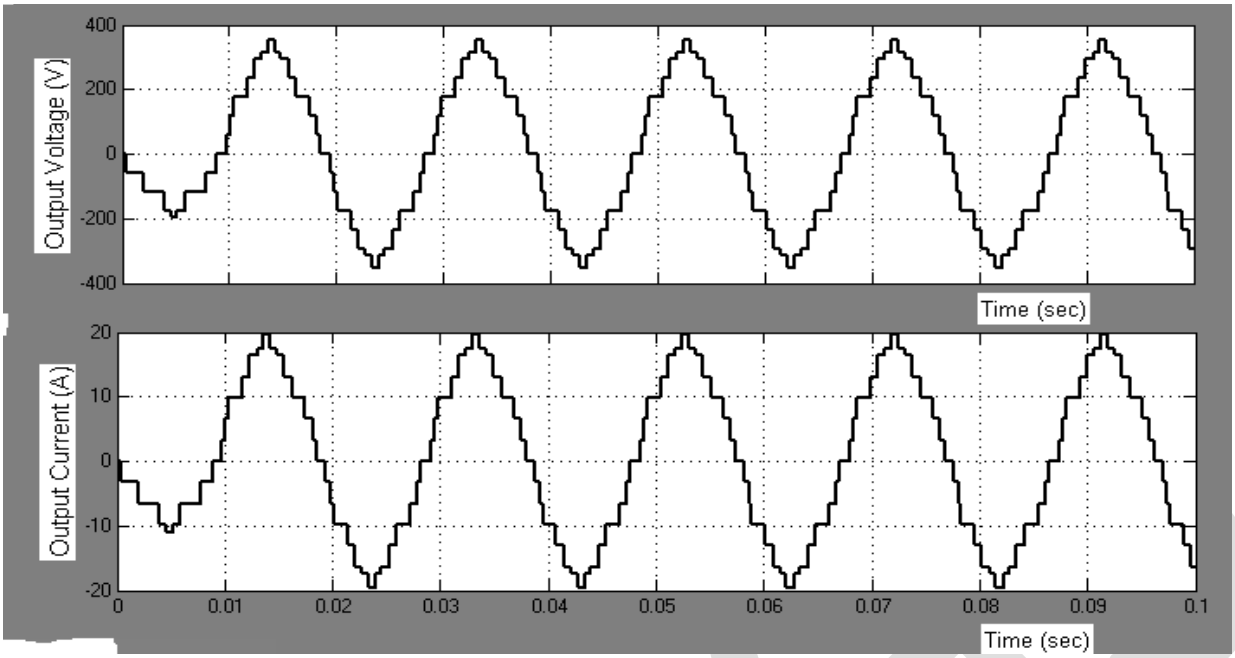

Fig 5: Output of 15 Levels multilevel Inverter

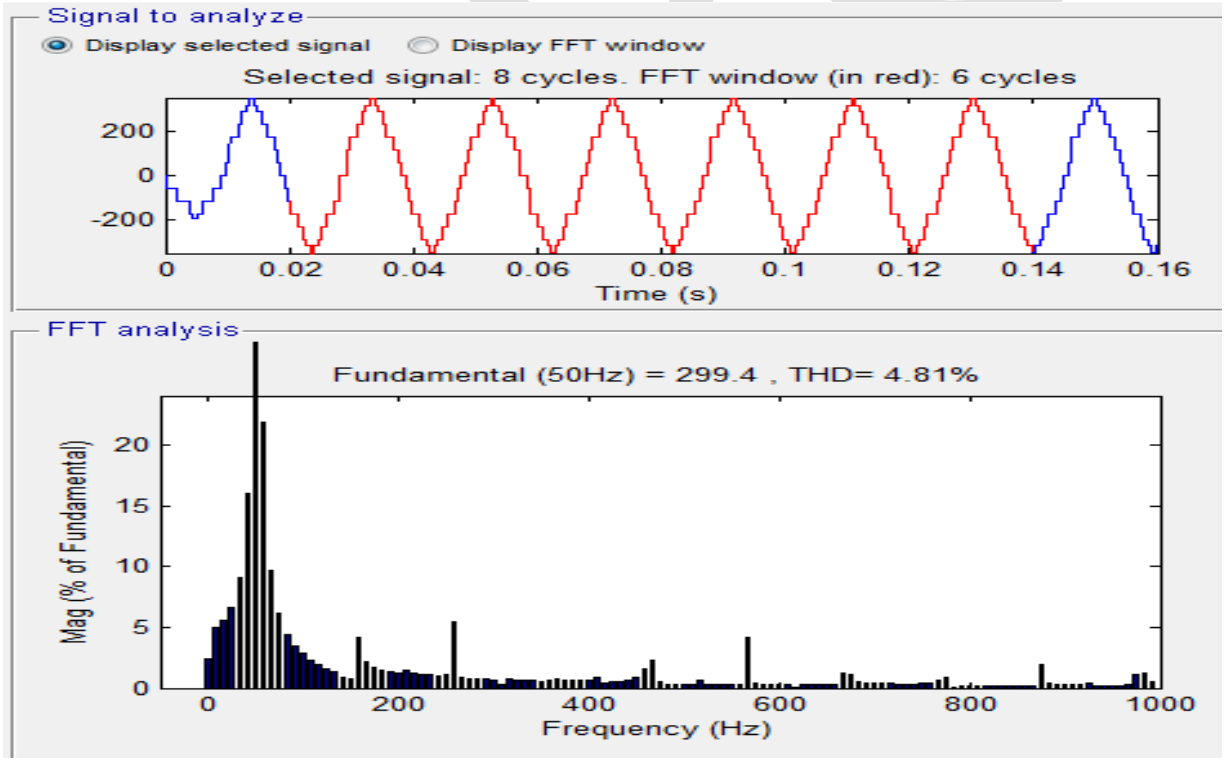

Fig 6: FFT Analysis of 15 Levels Multilevel Inverter

VI. CONCLUSION

Cascade NPC H-bridge topology is selected for implementing FIFTEEN-level inverter due to limitations of NPC and FC topologies .Low-switching frequency operation of multilevel inverters is essential to reduce the switching losses in medium voltage high power applications. Proposed SOP technique permits multilevel inverter to operate at an average device switching frequency limited to rated fundamental frequency without compromising on harmonic distortion. Optimal nine-level waveforms are produced using SOP technique and then switching instants for each semiconductor device is determined based on the criteria to reduce device switching frequency as well as to ensure minimal unbalance in the dc-link capacitor voltages. Experimental results for four different operating points demonstrate effectiveness of the proposed modulation in limiting average device switching frequency to rated fundamental frequency without compromising on THD as well as resulting in low ripple at dc-link voltages. Compared to other low-switching frequency control algorithms for nine-level inverter like model predictive control (*fs* = 425 to 500 Hz) [16] and adaptive duty-cycle modulation algorithm (*fs* = 285 to 785 Hz) [17], the switching frequency of operation has been reduced more than five times without compromising on THD of current waveforms.

REFERENCES:

[1]Amarendra Edpugantiand Akshay K. Rathore*,"* Optimal Low Switching Frequency Pulsewidth Modulationof Nine-Level Cascade Inverter" IEEE transactions on power electronics, vol. 30, no. 1, january 2015

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters -state of the art,challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581– 2596, Aug. 2010.

[3] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, and M. Pe´rez, J. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[4] M.Malinowski, K. Gopakumar, J. Rodriguez, and M. Pe´rez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[5] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral point- clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[6] J. Rodriguez, L. Franquelo, S. Kouro, J. Leon, R. Portillo, M. Prats, and M. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[7] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[8] J. Rodriguez, S. Bernet, B.Wu, J. Pontt, and S.Kouro, "Multilevel voltage source- converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[9] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999.

[10] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[11] S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kv neutral-point-clamped, flying-capacitor, and series-connected h-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, Jul/Aug. 2007.

[12] W. Hill and C. Harbourt, "Performance of medium voltage multi-level inverters," in *Proc. IEEE 34th Annu. Meet. Ind. Appl. Conf.*,, vol. 2, 1999, pp. 1186–1192.

[13] Z. Shu, X. He, Z. Wang, D. Qiu, and Y. Jing, "Voltage balancing approaches for diode-clamped multilevel converters using auxiliarycapacitor-based circuits," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp.2111–2124, May 2013.

[14] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamentalswitching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8,pp. 3482–3494, Aug. 2012.

[15] Z. Cheng and B. Wu, "A novel switching sequence design for five-level npc/h-bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2138–2145, Nov. 2007.

[16] Z. Du, L. Tolbert, B. Ozpineci, and J. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded h-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 25–33, Jan.2009.

[17] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded h-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2691–2699, Aug. 2010.

[18] S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced switching-frequency modulation algorithm for high-power multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2894–2901, Oct. 2007.

[19] H. S. Patel and R. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part i–harmonic elimination, "*IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 310–317, May 1973.

[20] H. S. Patel and R. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part ii—voltage control techniques, "*IEEE Trans. Ind. Appl.*, vol. IA-10, no. 5, pp. 666–673, Sep.1974.

[21] I. Pitel, S. N. Talukdar, and P. Wood, "Characterization of programmed waveform pulse width modulation," *IEEE Trans. Ind. Appl.*, vol. IA-16,no. 5, pp. 707–715, Sep. 1980.

[22] P. Enjeti, P. Ziogas, and J. Lindsay, "Programmed pwm techniques to eliminate harmonics: a critical evaluation," *IEEE Trans. Ind. Appl.*, vol.26, no. 2, pp. 302–316, Mar./Apr. 1990.
[23] A. Maheshwari and K. D. T. Ngo, "Synthesis of six-step pulse width modulated waveforms with selective harmonic elimination," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 554–561, Oct. 1993.
[24] F. Swift and A. Kamberis, "A new walsh domain technique of harmonic elimination and voltage control in pulse-width modulated inverters," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 170–185, Apr. 1993.
[25] T.-J. Liang, R. O'Connell, and R. Hoft, "Inverter harmonic reduction using walsh function harmonic elimination method," *IEEE Trans. Power Electron.*, vol. 12, no. 6, pp. 971–982, Nov. 1997.
[26] J. Chiasson, L. Tolbert, K. McKenzie, and Z. Du, "A complete solution to the harmonic elimination problem," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 491–499, Mar. 2004.
[27] J.Wells, B. Nee, P. Chapman, and P. Krein, "Selective harmonic control: a general problem formulation and selected solutions," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1337–1345, Nov. 2005.
[28] V. Blasko, "A novel method for selective harmonic elimination in power electronic equipment," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp.223–228, Jan. 2007.
[29] V. Agelidis, A. Balouktsis, I. Balouktsis, and C. Cossar, "Multiple sets of solutions for harmonic elimination pwm bipolar waveforms: analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 415–421, Mar. 2006.
[30] J. Wells, X. Geng, P. Chapman, P. Krein, and B. Nee, "Modulation-based harmonic elimination," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp.336–340, Jan. 2007.
[31] G. Poddar and M. Sahu, "Natural harmonic elimination of square-wave inverter for medium-voltage application," *IEEE Trans. Power Electron.*,vol. 24, no. 5, pp. 1182–1188, May 2009.
[32] J. Chiasson, L. Tolbert, K. McKenzie, and Z. Du, "A unified approach to solving the harmonic elimination equations in multilevel converters, "*IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 478–490, Mar. 2004.
[33] A. Kavousi, B. Vahidi, R. Salehi, M. Bakhshizadeh, N. Farokhnia, and S.Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 27, no.4, pp. 1689–1696, Apr. 2012.
[34] A. Rathore, J. Holtz, and T. Boller, "Generalized optimal pulse width modulation of multilevel inverters for low switching frequency control of medium voltage high power industrial ac drives," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4215–4224, Oct. 2013.
[35] A. Rathore, J. Holtz, and T. Boller, "Synchronous optimal pulse width modulation for low-switching-frequency control of medium-voltage multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2374–2381, Jul. 2010.
[36] T. Boller, J. Holtz, and A. Rathore, "Optimal pulse width modulation of a dual three-level inverter system operated from a single dc link," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 1610–1615, Sep./Oct. 2012.
[37] J. Holtz and N. Oikonomou, "Optimal control of a dual three-level inverter system for medium-voltage drives," *IEEE Trans. Ind. Appl.*, vol. 46, no.3, pp. 1034–1041, May/Jun. 2010.
[38] J. Holtz and B. Beyer, "Fast current trajectory tracking control based on synchronous optimal pulse width modulation," *IEEE Trans. Ind. Appl.*, vol.31, no. 5, pp. 1110–1120, Sep./Oct. 1995.
[39] J. Holtz and B. Beyer, "The trajectory tracking approach-a new method for minimum distortion pwm in dynamic high-power drives," *IEEE Trans. Ind. Appl.*, vol. 30, no. 4, pp. 1048–1057, Jul./Aug. 1994.
[40] J. Holtz and N. Oikonomou, "Estimation of the fundamental current in low-switching-frequency high dynamic medium-voltage drives," *IEEE Trans. Ind. Appl.*, vol. 44, no. 5, pp. 1597–1605, Sep./Oct. 2008.
[41] J. Holtz and N. Oikonomou, "Fast dynamic control of medium voltage drives operating at very low switching frequency - an overview," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1005–1013, Mar. 2008.
[42] N. Oikonomou and J. Holtz, "Closed-loop control of medium-voltage drives operated with synchronous optimal pulse width modulation," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 115–123, Jan./Feb. 2008.
[43] J. Holtz and N.Oikonomou, "Synchronous optimal pulse width modulation and stator flux trajectory control for medium-voltage drives," *IEEE Trans. Ind. Appl.*, vol. 43, no. 2, pp. 600–608, Mar./Apr. 2007.
[44] J. Holtz and B. Beyer, "Optimal synchronous pulse width modulation with a trajectory-tracking scheme for high-dynamic performance," *IEEE Trans. Ind. Appl.*, vol. 29, no. 6, pp. 1098–1105, Nov./Dec. 1993.
[45] J. Holtz, "Pulse width modulation for electronic power conversion," *Proc.IEEE*, vol. 82, no. 8, pp. 1194–1214, Aug. 1994.
[46] G. S. Buja, "Optimum output waveforms in PWM inverters," *IEEE Trans Ind. Appl.*, vol. IA-16, no. 6, pp. 830–836, Nov. 1980.
[47] T. Boller, J. Holtz, and A. Rathore, "Neutral point potential balancing using synchronous optimal pulse width modulation of multilevel in medium voltage high power ac drives," *IEEE Trans. Ind. Appl.*, vol. PP, no. 99, pp.1–1, 2013.
[48] J. Holtz and N. Oikonomou, "Neutral point potential balancing algorithm at low modulation index for three-level inverter medium-voltage drives, "*IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 761–768, May/Jun. 2007.
[49] H. du T. Mouton, "Natural balancing of three-level neutral-point-clamped PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1017–1025, Oct. 2002