

Low Voltage, Low Power Rail to Rail Operational Transconductance Amplifier with Enhance Gain and Slew Rate

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Abstract— Proposed paper deals with well-defined design criteria of rail to rail operational transconductance amplifiers. The system supply voltage is 1.6 V and the power consumption goes up to 15.03uW. The proposed amplifier was implemented in a 45nm-CMOS technology. Simulation results of proposed OTA achieves high 76.6 dB DC gain and slew rate 200 (V/us) with, 87.67dB PSRR and 82.66 dB CMMR.

Keywords— OTA, amplifier, transconductance, PSRR, CMRR, low voltage, RtR.

INTRODUCTION

Due to the highly demand of smaller area (size) and longer battery life for convenient applications in all marketing segments including consumer electronics, medical, computers and telecommunications low voltage and low power silicon chip design has been growing rapidly. To reduce current consumption and power consumption of the system the supply voltage is being scaled downward. The objective of this method is to implement the design of low power and low voltage op-amp for Telecommunications and Biomedical applications [1].

In design of most closed loop systems, design of the OTA is most challenging unit from design perspective. It has to achieve high DC gain and low thermal and flicker noise, also high band width required for systems with high frequency clock, especially in switched capacitor applications. Additionally, power consumption of the OTA is one of critical issues for applications with low power consumption target. Slew-rate and input common mode range are other important aspects of the OTA [2]. Telescopic and folded-cascode structures are two common structures for single stage opamps.

Two main drawback of first one are low input common mode range and large voltage headroom in output and main drawbacks of folded one is higher power consumption and lower UGBW. In this work to benefit high input common mode range of folded-cascode and also having higher DC gain and UGBW, total transconductance of the amplifier is increased adding extra paths for signal from input to output [3].

Other techniques for increasing DC gain of the op-amp such as using positive feedback or gain boosting are based on increasing output resistance of the op-amp and so only DC gain of the op-amp increases with these techniques and UGBW remains constant [4]-[5]. The OTA is an amplifier without buffer at output stage drives only load. Which is called as VCCS because its differential input voltage produces a current at output stage.

OTA is the backbone of analog circuits. OTA faces many difficulties with low voltage design providing high gain and low power consumption [6]. To improve the gain, of cascoded transistors is not easy for low voltage and low power design due to its output swing restriction. The current equation of OTA is shown in below which signifies that the transconductance of design is highly depends on the biasing current [7]

$$I_o = G_m \{V(+)-V(-)\}$$

The proposed amplifier has giving better performance and consuming a fraction of the power at less supply voltage.

The design procedure is based on following main parameters: noise, phase margin, gain, load capacitance, slew rate(SR), input common mode range, common mode rejection ratio(CMRR)and power mode rejection ratio (PSRR) with less power consumption.

PROPOSED METHODOLOGY

As the input stage, the differential amplifier is used for operational amplifiers .the problem is that it behaves as a differential amplifier only over a limited range of common –mode input. Therefore, to make the operational amplifier versatile, its input stage should work for RtR common- mode input range .the most common method to achieve this range is to use a complementary differential amplifier at the input stage. Where N1, N2 and P1, P2 constitute the n- type and p-type differential input pairs, respectively.

The N-MOS differential pair is shown in fig 1.in which input pair, N1 & N2, is able to reach the positive supply rail. The range extends from the positive supply to $(V_{gs, n} + V_{Dsat, b})$ above the negative supply. This minimum voltage is needed to keep the NMOS differential pair and the tail current source in saturation. The role of tail current source is to suppress the effect of input CM level variations on the operation of N1 and N2 and the output level .A similar analysis can be carried out for the PMOS differential pair.

The proposed circuit is shown in fig. 2. RtR input means that input signal can be anywhere between the supply voltages with all the transistors in the saturation region.

To have a RtR common mode input range, two complementary differential pairs are required to form the input stage .N- channel input pair,N1 & N2, is able to reach the positive supply rail while the P- channel input pair, P1 & P2, is able to reach the negative supply rail.

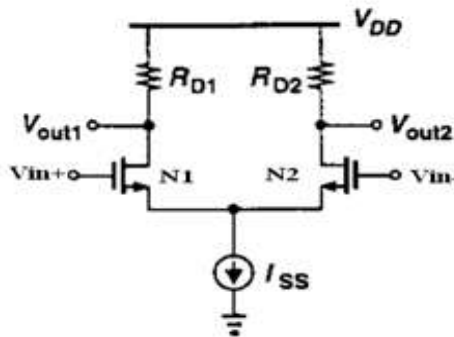


Fig.1 NMOS differential pair

The constant-gm control circuit is achieved through transistor N3-N6 and P3-P6.this circuit maintains a constant tail current when either of the two differential pairs goes off. V_{bn_tail} and V_{bp_tail} is the control voltage of N3 and P3 MOSFET.

$$g_{m, np} = g_{m, n} + g_{m, p}$$

$$g_{m, n} = \sqrt{2\mu_n C_{ox}(W/L)I_D}$$

Where $g_{m, n}$ and $g_{m, p}$ are the transconductance of NMOS and PMOS respectively.

In order to describe the operation of constant $-gm$ control circuit, first, it is supposed that PMOS and NMOS differential pairs are both in operation and the transistor P3 and N3 as the tail current source provide the same current for PMOS and NMOS differential pairs respectively.

The constant gm circuit (P4-P6) and (N4-N6) are used to control transconductance. Through adjusting the ratio of width to length of the input differential pairs, the tail current can be kept constant and stable. The input differential pairs are kept biased in saturation region under all conditions [18].

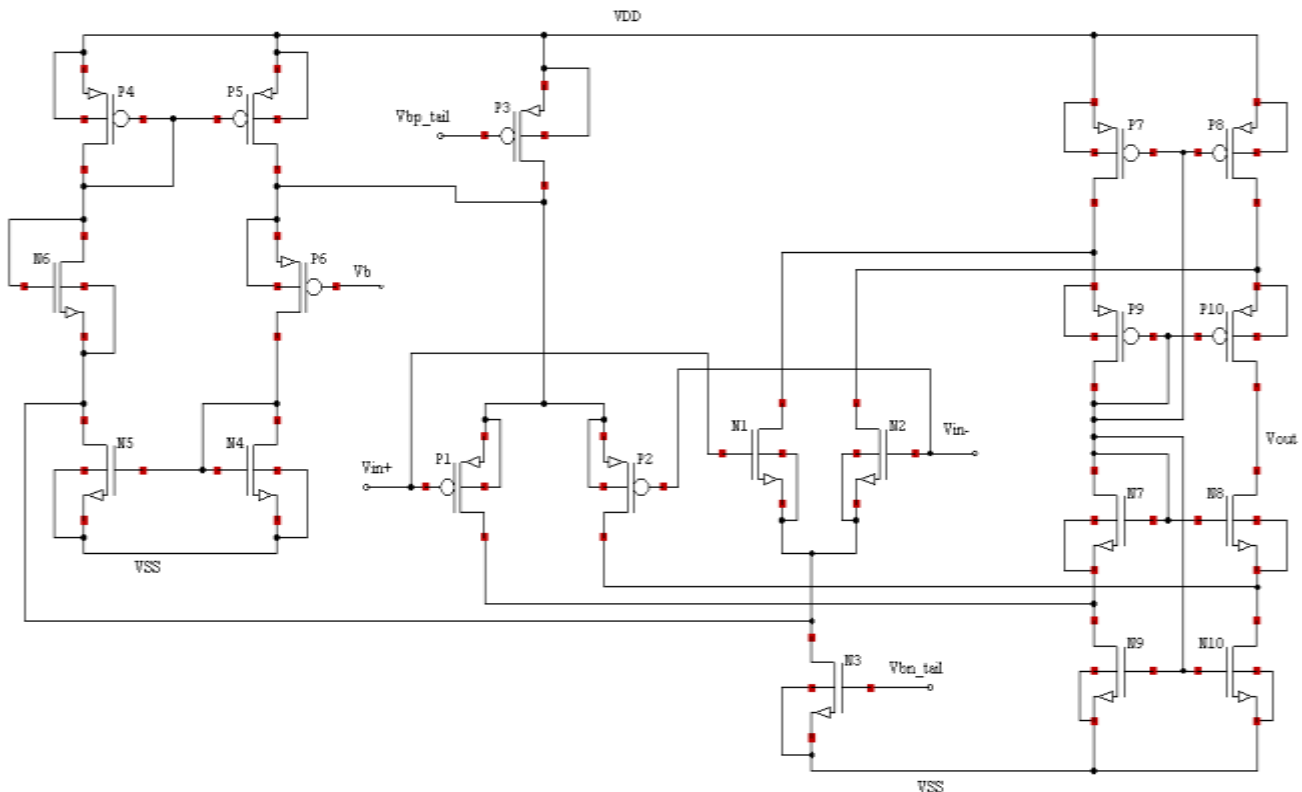


Fig .2 Proposed rail to rail OTA

SIMULATION AND RESULT

The proposed rail to rail operational transconductance amplifier is operates with 1.6v power supply and fabricated in a standard 45nm CMOS process with 9.04uA current consumption. The proposed amplifier has giving better performance and consuming a fraction of the power 15uW at less power supply.

The gain of proposed RtR is 76.6 dB, phase margin 38.03 (deg), slew rate is 200(V/us), CMRR is 82.66dB and PSRR is 87.67 dB. Simulation result summary is shown in below table I.

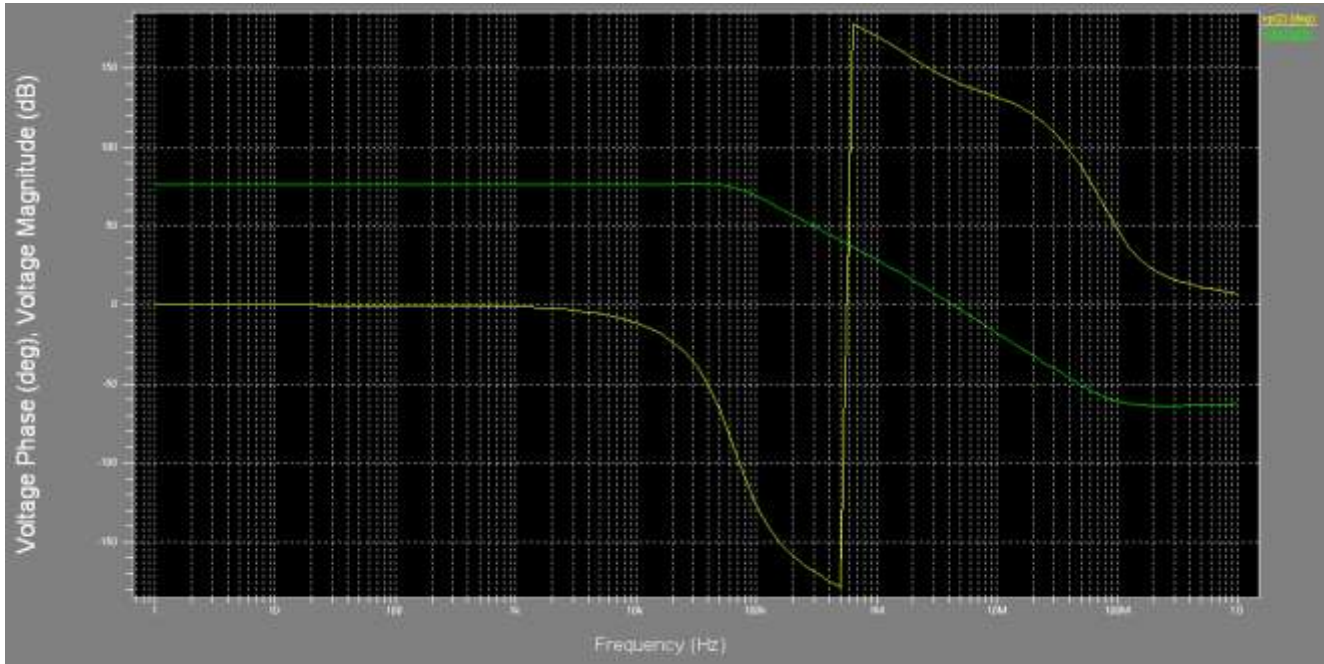


Fig.3. Gain (dB) and Phase Margin (deg) Versus Frequency (Hz)

Table I
Simulation Result Summary

Design	Result
technology	45nm
Slew rate(V/us)	200
CMRR(dB)	82.66
Gain(dB)	76.6
Phase margin(deg)	38.03
Supply voltage	1.6v
Figure of merit(FOM) (MHZpF/mA)	3676.59
Maximum output current (uA)	4.1
PSRR(dB)	87.67
Power consumption (uW)	15.04
GBW(MHz)	331.2

CONCLUSION

Operational amplifiers input stages utilize a single differential pair have a common mode input range that extends to only one rail. This limits the application of operational amplifiers. An RtR common mode input range is a desirable characteristic for the input stage which makes op-amp more versatile. This characteristic can be achieved using a compound differential pair structure called the complementary differential pair (both NMOS and PMOS differential pair).

The proposed RtR OTA does not require an extra circuit which reduces design complexity, area and power consumption. It has been demonstrated that the proposed circuit can boost the gain, phase margin, slew rate, CMRR, PSRR using 1.6 supply voltages.

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