Fault Tolerant Over Hardware Efficient FIR Filter

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Abstract— In today's world there is a great need for the design of low power and area efficient high performance DSP system.FIR filter is considered to be the fundamental device in the broad application of wireless as well as the video and image processing system. With the aim of getting the reliable operation, these filters are protected using the Error correction Code. The pipelined FIR filter design which reduces the critical path by interleaving the pipelined latches along the datapath, with the sense of increasing the number of latches and then the system latency. But the parallel processed FIR filter design increases the sample rate thereby replicating the hardware, so that the multiple number of inputs gets processed parallely and at the same time generating multiple number of outputs with the disadvantage of increased area in the design. To overcome this disadvantage and in the sense of retaining these such advantage of parallel processing,the hardware efficient filter structure is to be proposed, and these filter structure is to be recovered from error by the application of Error Correction Code.

Keywords— FIR filter, Error Correction Code, Parallel Processing.

INTRODUCTION

The Digital Filters plays a vital role in the analog and digital communication. The main purpose of using the filters is to eliminate the undesired signal components thereby providing the better quality signal at the output. The digital filters having the unique characteristics of generating the stabilized signal at the output while compared with the analog filters. So that the digital filters are more preferable than the analog one. There are two main kinds of digital filters they are 1.FIR (Finite Impulse Response) and 2.IIR (Infinite Impulse Response) filter. The FIR filter is preferred over the IIR filter because of efficient hardware implementation with fewer precision errors and also giving the stabilized response with the linear phase [1],also helps to know more about parallel processing.

The Pipelining as well as the Parallel Processing techniques can reduce the power consumption by lowering the supply voltage when the sampling speed does not increase. In order to reduce the large amount of hardware cost a new technique is being proposed called as the Iterated Short Convolution Algorithm (ISC) [2].This ISC based technique is being transposed to get the hardware efficient FIR Filter structure. This technique is highly effective when the length of the FIR filter is large. This method is based on the mixed radix algorithm and the fast convolution algorithm. The application of Error Correction Code is being briefly studied using [3].One beneficial method that the exchange of adders with the multipliers because the adders which are weighing less as compared with the multipliers in case of silicon area [4].This proposed filter structure exploits the symmetric filter coefficients thereby reducing the number of multipliers in the sub filter section with the expense of increasing the additional adders in the pre-processing and post processing blocks.
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The FFA based FIR filter structure having the additional pre-processing and post processing blocks, these adders mainly uses the full adder with the ripple carry adder which causes more timing delay because of taking longer time to execute the program [5].So to overcome that the ripple carry adders are replaced with the carry save adder in order to provide efficient hardware structure thereby reducing the timing delays has been proved. A new efficient FIR filter implementation as been proposed to reduce the hardware cost. For that they are considering the two contributions:1.The filter spectrum characteristics are being exploited in order to select the fast filter structure,2.Introduction of Novel block filter quantization algorithm is introduced [6].These technique which reduces the number of binary adders upto 20%.

The DSP system is used for further hardware efficient operation designing the system with multiplier less implementation of DSP system. This system effectively replaces all the multipliers and adders into the Look Up table (LUT) and Shifter-accumulator thereby saving more hardware space [7].The significant improvement in area, power and delay can be achieved by using the truncated multipliers. In this proposed technique the LSB bits in the output are operated with the operation of deletion, reduction, truncation,

rounding and final addition.So.here there is no requirement for the error compensation circuits [8].The multiplier in the filter design is replaced with the shifter and adder. These shifter and adder in the design which enhances the performance of the system thereby reducing the unwanted additions in order to reduce the switching power dissipation [9] to enhance the performance. The error correction technique in the design is used to provide the realiable signal at the output.

In this brief, this paper helps to provide the error corrected hardware efficient filter structure with the modification in the filter convolution structure as compared with the traditional FIR filter convolution. This paper helps to maintain the constant pre-processing and post processing blocks at the same time to minimize the number of multipliers in the efficient filter design.

II.EXISTING FILTER STRUCTURE

The existing parallel filter structure is shown in the Fig.1.The filter structure is designed for four input and four coefficients. The four filter inputs are considered to be x(4k), x(4k+2),x(4k+3) and x(4k+1) and the filter coefficients are considered to be h0,h1,h2 and h3.The generated outputs are found to be y(4k), y(4k+2),y(4k+3) and y(4k+1).

A.Original Module

The original module should be represented in the Fig.1.In this module the applied input gets convoluted by using its filter coefficients then it generates the convoluted output. The original module operates on the equation (1) given below.

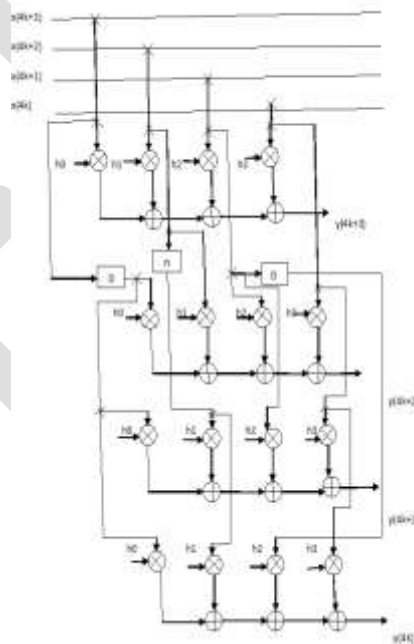$$y[n] = \sum_{l=0}^{\infty}(x[n-l])\,h[l] \qquad (1)$$

Fig.1.Existing Filter Structure

B.Redundant Module

The redundant module is the module used for achieving the reliable operation over the original module. The redundant module is said to be the parity module which is used to generate the parity bits. These parity bits are represented as y(3k),y(3k+1) and y(3k+2).The module takes a block of k bits and generated the block of n bits and the parity is obtained as n-k bits. The Parity check bit equations are given in (2).

$$p1 = d1 \pm d2 \pm d3$$

$$p2 = d1 \pm d2 \pm d4 \qquad (2)$$

$$p3 = d1 \pm d3 \pm d4$$

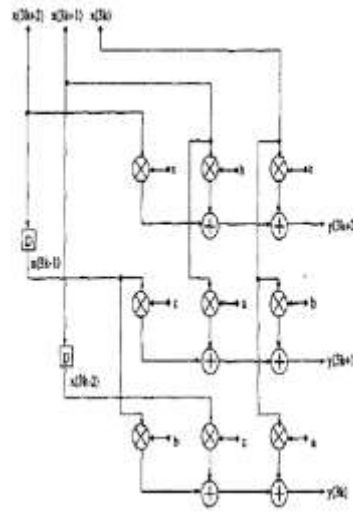The redundant module is shown in the Fig.2

Fig.2 Redundant Module

C. Single Error Correction Code

The single error correction module is used to correct the single bit error in the generated or convoluted output at the original module. By applying the parity over the original module the error in the bit at the convoluted output is to be detected and corrected with the help of equation (3).

$$Z1[n] = \sum_{l=0}^{\infty}(x1[n-l] + x2[n-l] + x3[n-l])h[l]$$

$$Z2[n] = \sum_{l=0}^{\infty}(x1[n-l] + x2[n-l] + x4[n-l])h[l] \qquad (3)$$

$$Z3[n] = \sum_{l=0}^{\infty}(x1[n-l] + x3[n-l] + x4[n-l])h[l]$$

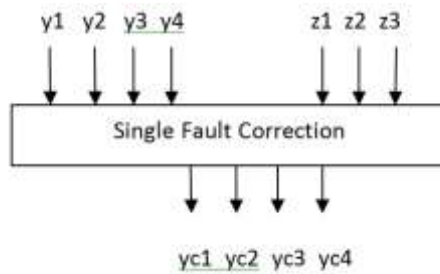The single error correction module is given in the below Fig.3.

Fig.3.Single error correction module

III.PROPOSED FILTER STRUCTURE

The proposed filter structure has a difference in the adder structure implementation as compared with the existing parallel filter structure. This efficient adder structure implementation in the parallel filter is given in the Fig.4.
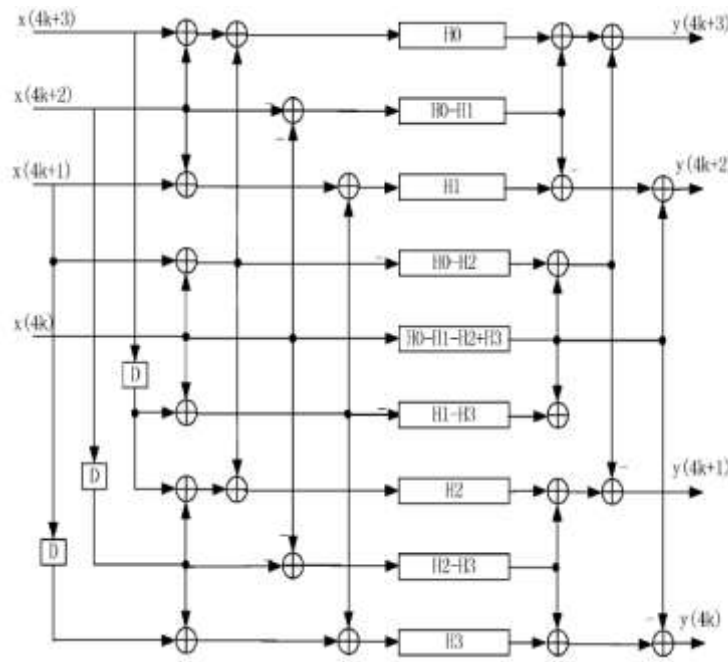

Fig.4 Proposed Hardware efficient filter

A. Original Module

The original module is represented in the Fig.4.In this module the applied input gets convoluted by using the efficient adder structure.

B.Redundant Module

The redundant module is same as that of the existing systems redundant module used for achieving the reliable operation over the main module. This module is used for generating the parity bits also represented as z1, z2 and z3.The parity is calculated as n-k bits. Let us consider a simple example of Hamming code with k=4 and n=7,here the parity bits p1,p2 and p3 are computed based on the data bits d1,d2,d3 and d4 as follows:

$$p1 = d1 \pm d2 \pm d3$$

$$p2 = d1 \pm d2 \pm d4$$

$$p3 = d1 \pm d3 \pm d4$$

C.Single Error Correction Module

The single error correction module is used to correct the single bit error in the generated convoluted output at the proposed area efficient adder structure. The single error correction module is shown in the Fig.5.
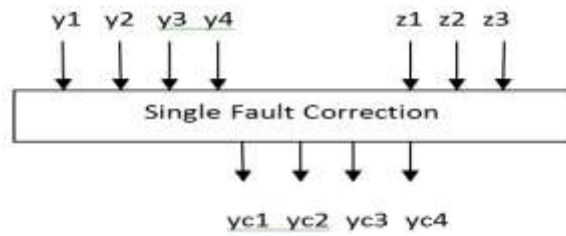
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Fig.5 Single error correction circuit

IV.SIMULATION RESULTS

The Simulation results and the RTL schematic for the existing and proposed module are given below:
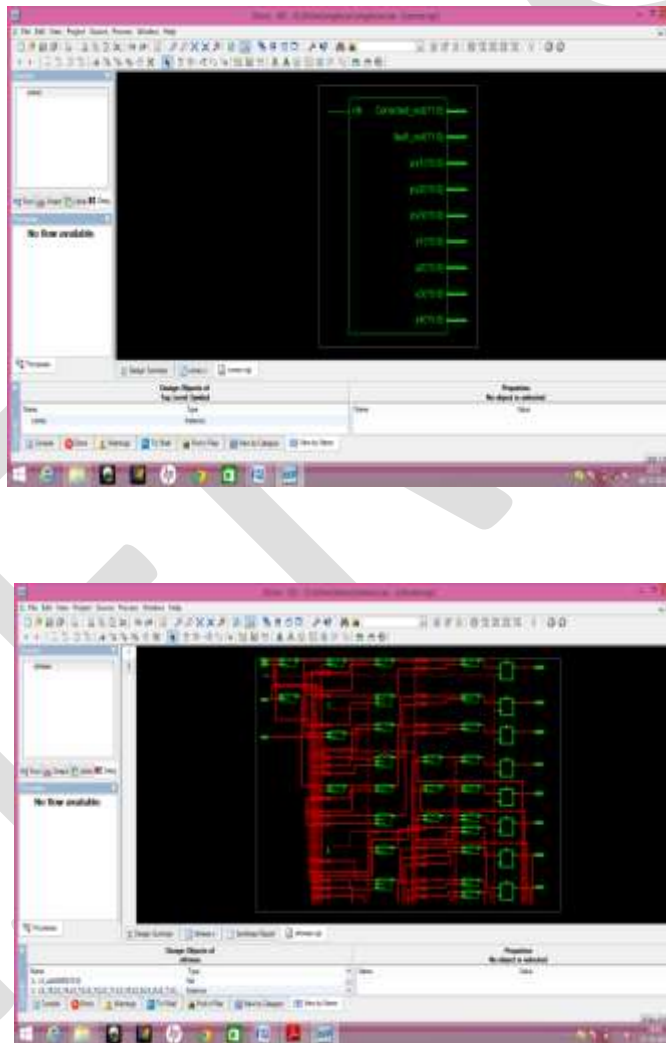

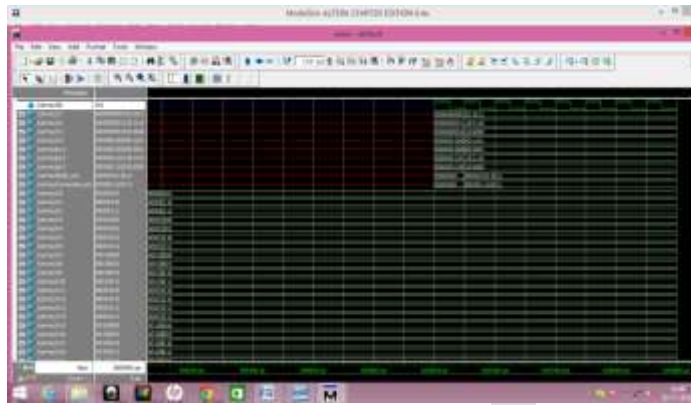Fig.6. RTL schematic view proposed filter structure
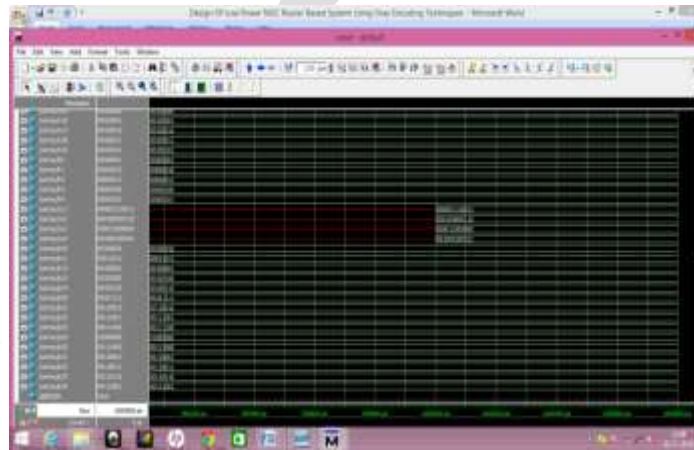
Fig.7.Output window with parity

Fig.8 Output window with error correction circuit.

Table 1. Comparison table for Existing and Proposed Blocks

	Unprotected Filter	Existing Module	Proposed Module
Slices	2061	2072	2053
LUT's	1211	1227	1202
Flipflops	5124	5134	5112
Gclk's	8%	12%	4%
No.of bonded IOB's	13%	18%	10%
Power(mW)	315	320	312
Time period(ns)	43.67	45.89	40.98

The proposed module is simulated using ModelSim XE simulator

V.CONCLUSION

In this paper, the Filter is designed with efficient hardware implementation structure for getting the reduced power with reduced hardware cost. The modified filter structure generates the similar result as that of the existing module. The power consumption should be reduced from 320mW to 312mW.The resource utilization can be obtained by analyzing the slices,flipflops,used gate clk's,and IOB's.The single bit error correction is achieved by using the Hamming Error Correction Code in the proposed system.

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