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Design of Low-Voltage and low-Power inverter based Double Tail Comparator

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ABSTRACT: Design of low voltage double-tail Comparator with pre-amplifier and latching stage is reported in this paper. Design has specially concentrated on delay of both single tail comparator and double-tail comparator, which are called clocked regenerative comparator. Based on a new dynamic comparator is proposed, where the circuit of conventional double tail dynamic comparator is modified for low power and fast operation even in small supply voltages. Simulation results in 0.25µm CMOS technology confirm the analysis results. It is shown that proposed dynamic comparator both power consumption and delay time reduced. Both delay and power consumption can be reduced by adding two NMOS switches in the series manner to the existing comparator. The supply voltages of 1.5V while consuming 15µw in proposed comparator and 16 µw in existing comparator respectively.

Keywords-Conventional dynamic comparator, double tail comparator, Proposed dynamic comparator, low power, fast operation, low power, Delay.

1.Introduction

Comparator is one of the fundamental building blocks in Analog-to-digital converters. designing high speed comparator is more challenging when the supply voltage is smaller. in other words to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Developing a new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low voltage operation, especially if they do not increase circuit complexity.

Additional circuitary is added to the conventional dynamic comparator to enhance the comparator speed in low voltage operation. Many high speed ADC's such as flash ADC's requires high speed, low power comparators with small chip area.a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

*2.*Conventional Single tail comparator

The schematic diagram of the conventional dynamic comparator. It is widely used in A/D converters. With high input impedance, rail-to-rail output swing, no static power consumption.

2.1.Operation

Two modes of operation reset phase and comparison phase. in reset phase clk=0,Mtail=off, reset transistors M7-M8 are ON, pull both output nodes to VDD to define start condition and have valid logical level. during the rest phase. in the comparison phase clk=VDD, Mtail=ON, reset transistors M7-M8 are OFF. Output nodes had been pre-charged to VDD, start to discharge with different rates depending on the corresponding input voltages. Where VINP>VINN, outp discharges faster than outn, where outp is(Discharged by transistor M2 drain current) falls down to before outn(discharged by transistor M1 drain current)the corresponding PMOS transistor M5 will turn ON initiating the latch regeneration caused by back-to-back inverters(M3,M5,M4,M6).Thus outn pulls to VDD and outp discharges to ground. If VINP<VINN, The circuit works vice versa. the delay of the comparator is comprised two delays t0 and tlatch.

$$t_0=\frac{C_L|V_{thp}|}{I2}\cong\frac{2C_L|V_{thp}|}{I_{tail}}\quad\ldots\ldots\ldots(1)$$

where $I2=\frac{I_{tail}}{2}$+Iin,I2 can be approximated to be constant and equal to the half of tail current.

$t_{latch} = \frac{CL}{gm,eff} . \ln\left(\frac{\Delta Vout}{\Delta V0}\right) = \frac{CL}{gm,eff} . \ln\left(\frac{VDD/2}{\Delta V0}\right)$.....(2)

where gm,eff is the transconductance of the back-to-back inverters. In fact, this depends in logarithmic manner, on the initial output voltage difference at the beginning of the regeneration(i.e.t=t0),$\Delta V0$ can be calculated from

$$\Delta V0 = |Voutp(t = t0) - Voutn(t = t0)|$$

$$= |Vthp| - \left(\frac{I2t0}{CL}\right) = |Vthp|\left(1 - \frac{I2}{I1}\right) \text{.....(3)}$$

The current difference ΔIin=|I2-I1|,between the branches is much smaller than I1 and I2,thus I1 can be approximated by Itail/2 and (3) can be written as

$$\Delta V0 = |Vthp|\frac{\Delta Iin}{I1}$$

$$\approx |Vthp|\frac{\Delta Iin}{Itail}$$

$$= 2|Vthp|\frac{\sqrt{\beta 1,2 Itail}}{Itail}.\Delta Vin$$

$$= 2|Vthp|\sqrt{\frac{\beta 1,2}{Itail}}.\Delta Vin \text{.....(4)}$$

In this equation input transistors current factor and Itail is a function of input common mode voltage(Vcm) and VDD. Now substituting ΔV0 in latch delay expression and considering t0,the expression for the delay of the comparator as

tdelay=t0+tlatch

$$= \frac{CL|Vthp|}{I2} + \frac{CL}{gm,eff} . \ln\left(\frac{VDD}{4|Vthp|\Delta Vin}\right)\sqrt{\frac{Itail}{\beta 1,2}} \text{.....(5)}$$

Total delay is directly proportional to the comparator load capacitance CL, and inversely proportional to the input voltage difference(ΔVin),besides the delay depends indirectly to the input common mode voltage(Vcm). By reducing Vcm, the delay t0 of the first sensing phase increases because lower Vcm causes smaller bias current(Itail),on the other hand, shows that delay discharge with smaller tail results in an increased initial voltage difference(ΔV0),reducing tlatch.

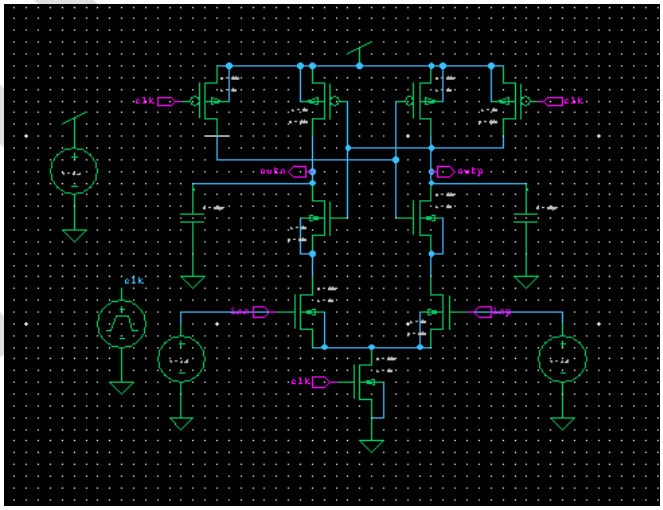


Fig2.1.Schematic diagram of single-tail dynamic comparator.

3.Conventional Double-tail Dynamic Comparator

A Conventional double tail comparator is shown in fig2.it can operate lower supply voltages compared to the single tail comparator. The double tail enables both large current in the latching stage and wider Mtail2,for fast latching independent on input common mode voltage(Vcm),and a small current in the input stage(small Mtail1),for low offset. input and ground of the circuit based on the tail current. Intermediate stage transistor is switching when voltage drop occurs at the nodes fp and fn.

3.1.Operation

Fig2.shows the operation of conventional double-tail dynamic comparator.The intermediate stage formed by MR1 andMR2 passes Δfn/fp to the cross-coupled inverters formed by good shielding between input and output, resulting reduced value of kick-back-noise.

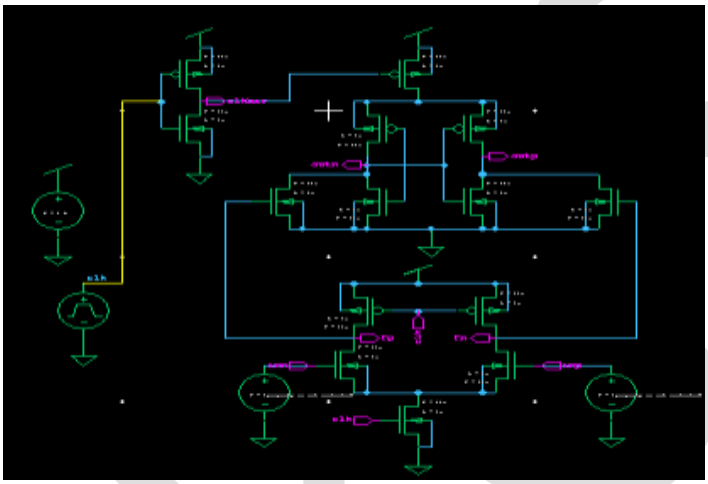


Fig3.1. Schematic diagram of Conventional Double-tail dynamic comparator.

4.Modified Existing dynamic comparator(main idea)

Fig4.shows operation of modified existing comparator (main idea).it gives better performance in low voltage applications, and it is designed based on the double-tail structure. latch regeneration speed is increased by increasing Δfn/fp. Two control transistor(MC1 and MC2) have been added to the first stage in parallel to M3/M4 transistors but in cross coupled for the purpose of increasing speed.

4.1Operation

During the reset phase clk=0,tail transistors Mtail1 and Mtail2 are off, avoiding the static power,M3 and M4 pulls both fn and fp to VDD, then the control transistors MC1 and MC2 are in cutoff stage.MR1 and MR2 are intermediate transistors, it reset both latch outputs to ground. During the comparison phase, clk=VDD,Mtail1 and Mtail2 are ON, transistors M3 and M4 are turn off. at the beginning of this stage the control transistors MC1 and MC2 are still off. Thus the output nodes fp and fn start to drop different rates according to the input voltages. If VINP>VINN, fp discharges faster than fn, because transistor M2 provides more current than transistor M1.as long as fn continues falling the corresponding PMOS transistor MC1 start to turn on, pulling fp node back to VDD. So another control transistor MC1 remains turn off. it allowed fn to be discharged completely. When one of the control transistor turns ON, a current from VDD is drawn to ground via input and tail transistor, resulting in static power consumption. To overcome this issue, two NMOS switches are used below input transistors shown in fig 4.2.during the decision making phase, clk=VDD,Mtail1 and Mtail2 are ON, both NMOS switches are closed. Output node fn and fp are start to discharge with different rates, the comparator detects faster discharging node. Control transistors increase their voltage difference. Suppose that fp is pulling to VDD, fn should discharges completely. hence the switch in the charging path of fp will be opened, but other switch is connected to fn will be closed to allow the complete discharge of fn node. The operation of the control transistors with the switches emulates the operation of latch.

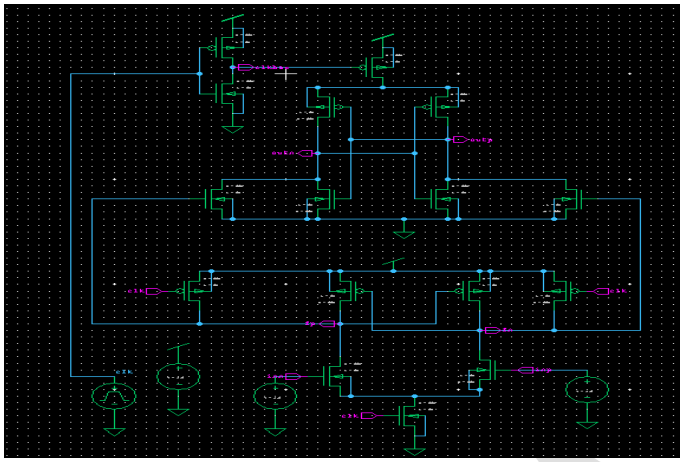


Fig4.1. Schematic diagram of Modified existing dynamic comparator(main idea)

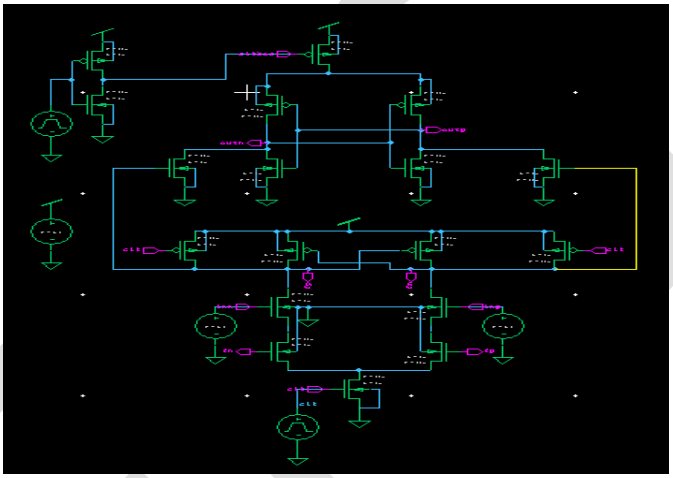


Fig4.2. Schematic diagram of Modified existing dynamic comparator(Final structure)

5.Proposed Double-Tail Dynamic Comparator

Fig5.shows the schematic diagram of Proposed comparator .it is designed based on the existing comparator. compared with proposed it provides, better performance of double tail comparator in low voltage applications. Drawback of Existing comparator is ,the nodes f_n and f_p starts to drop with different rates according to the input voltages. The continues falling of fn, the corresponding transistor M_{C1} starts to turn on and f_p node backs to V_{DD}. Node fn to be discharged completely(M_{C2} off).When one of the control transistors (M_{C1}) turns ON, a current from V_{DD} is drawn to the ground via input and tail transistor. Resulting a static power consumption. For this purpose two switching transistors (M_{sw3} and M_{sw4}) have been added to M_{sw1} and M_{sw2} in series manner. Proposed comparator reduced the delay, area and power.

5.1.Operation

Operation of Proposed in both reset and comparison phase is similar as Existing comparator .At the beginning of the decision making phase, both f_n and f_p nodes have been pre charged to V_{DD}. in the reset phase switches are closed , f_n and f_p starts to drop with different discharging rates. As soon as comparator detects that one of the f_n/f_p nodes is discharging faster, control transistors will act in a way to increase their voltage difference. If f_p is pulling up to V_{DD} and f_n should be discharged completely , hence switching in the charging path of f_p will be opened but the other switch connected to f_n will be closed to allow the complete discharge of f_n node. The operation of the control transistors with the switches emulates the operation of the latch.

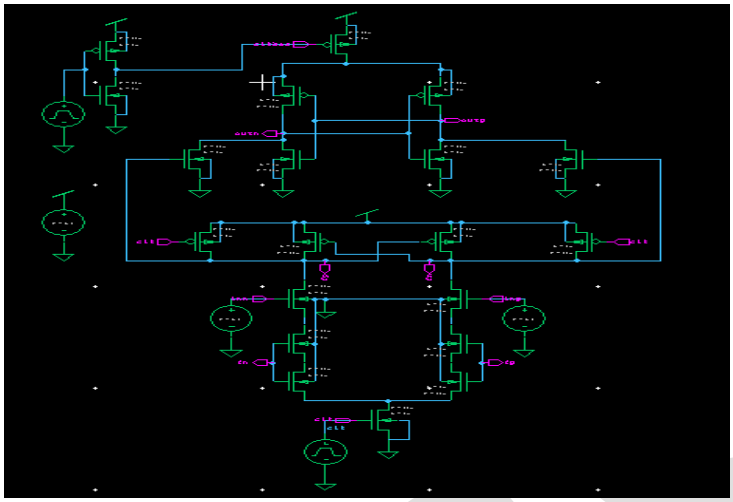


Fig5.1. Schematic diagram of Proposed dynamic comparator

6.Results

Fig6.1 Conventional single tail Comparator Simulation Results

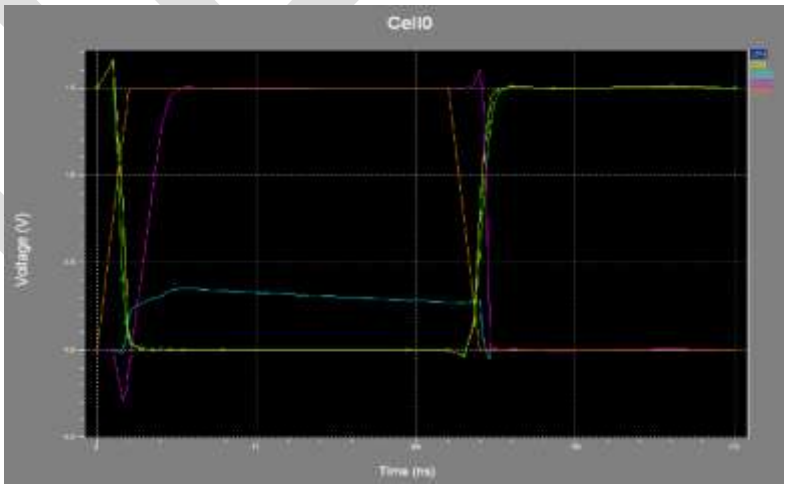


Fig6.2.Conventional double tail Comparator Simulation Results

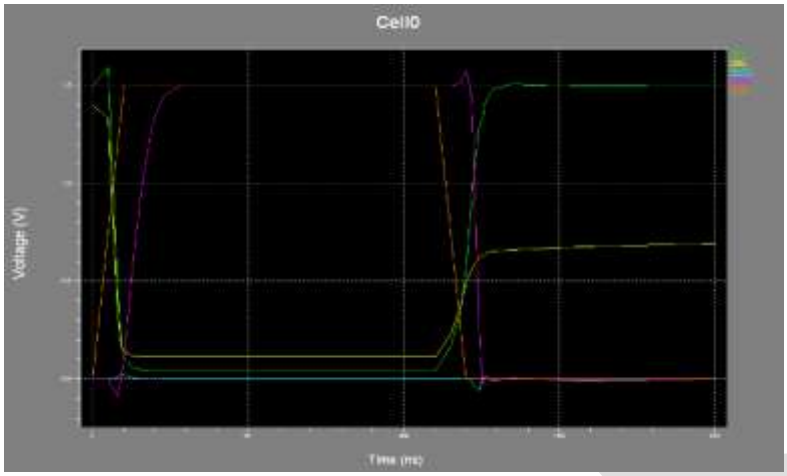


Fig6.3Modified existing Comparator(main Idea)Simulation Results

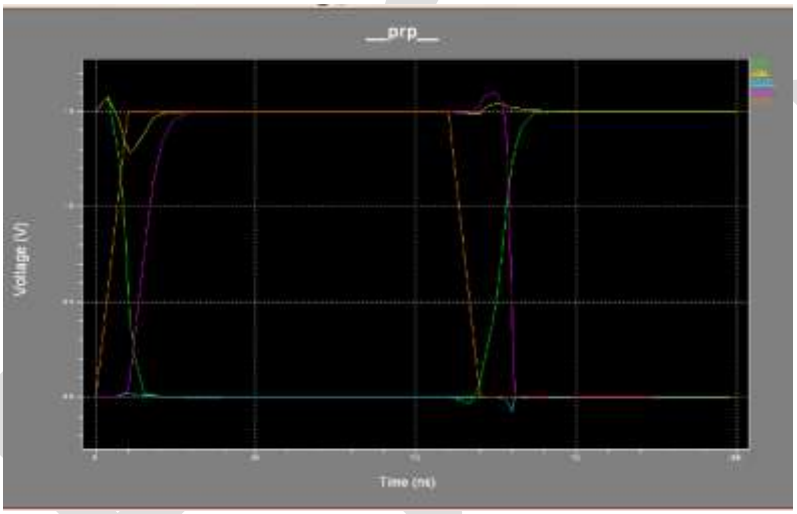


Fig6.4.Modified existing Comparator(Final structure)Simulation Results

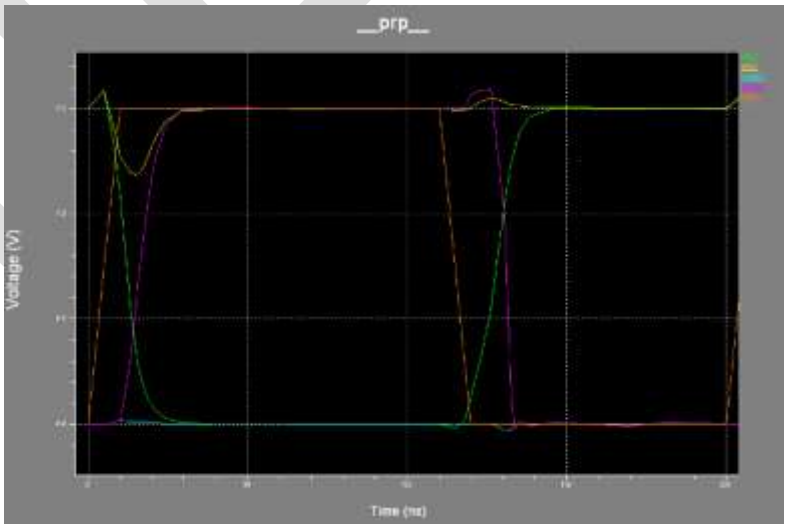
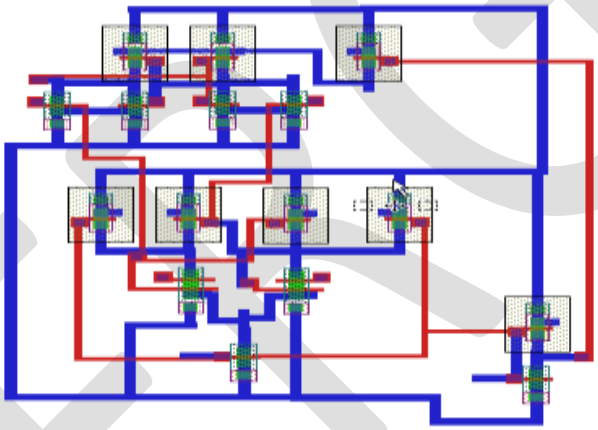


Fig6.5.ProposedComparator (Final structure) Simulation Results

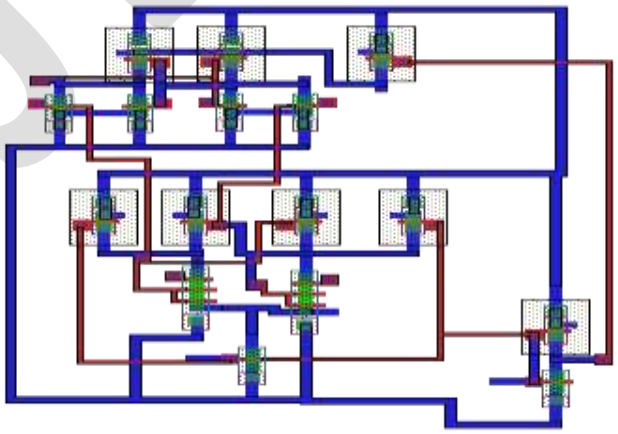
6.6.Performance Comparison Table:

Comparator Structure	Conventional Dynamic Comparator	Double tail Dynamic Comparator	Existing Dynamic Comparator	Proposed Comparator
Technology(CMOS)	250nm	250nm	250nm	250nm
Supply Voltage	5V	1.5V	1.5V	1.5V
Delay	25ns	1.1ns	12.22ns	11.34ns
Average Power	1.9mw	10 µw	16µw	15 µw

7.Layout design of the existing Comparator



8.Layout design of the Proposed Comparator



9.CONCLUSION

In this Paper we presented a comprehensive delay analysis for conventional dynamic comparator expression were derived. A new double tail dynamic comparator with two NMOS Switches was proposed in order to improve the performance of the comparator and no static power consumption. Pre layout simulation results in 0.25µm CMOS technology confirmed that the delay and energy per conversion of Proposed comparator is reduced.

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