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Analysis and Design of Low Voltage Low Power Dynamic Comparator with Reduced Delay and Power

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Abstract— High speed devices such as ADC, operational amplifier are of great importance and for this high speed application a major thrust is given towards low power methodologies. Reduction of power consumption in these device can be achieved by moving towards smaller feature size processes. Now ADC requires lesser power dissipation, low noise, better slew rate ,high speed etc. Dynamic comparator are being used in today's A/D converters extensively because these comparator are high speed ,consumes lesser power dissipation ,having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back to back inverter in these dynamic comparator provides positive feedback mechanism which convert a smaller voltage difference in full scale digital level output. A pre-amplifier based comparator can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise. However the pre-amplifier based comparator suffer large static power consumption as well as from the reduced intrinsic gain with the reduction of the drain to source resistance due to continuous technology scaling. In this paper a delay analysis has been presented for different dynamic comparators and finally a proposed designed has been given where delay has been reduced 264Ps and average power dissipation has been reduced to 1.09µw.The above design has been simulated in 180nm technology with a supply voltage of 0.8v

Keywords— High speed analog-to-digital comparators(ADCs) , Dynamic clocked comparator, low power analog design , Double-tail dynamic comparator, conventional dynamic comparator , preamplifier based comparators

INTRODUCTION

Comparator is a fundamental building block in analog-to-digital converter(ADCs). In design of ADCs , comparator of high speed , low power consumption are used. comparator in ultra deep sub micrometer (UDSM) technologies suffers from low supply voltage. hence design of high speed comparator is a challenge when the supply voltage is low[1]. Hence to achieve high speed in a given technology more transistor are required and more area and power is required. Technique such as supply boosting method[2],[3] a technique such as body driven transistor[4] ,[5] has been developed to meet the low voltage design. In addressing switching problems and input range two technique such as boosting and bootstrapping are used . In this paper the delay has been presented for various dynamic comparator architecture. Based on the double-tail architecture a new dynamic comparator has been presented where delay is comparatively reduce compared to the earlier design which doesn't require boosted voltage . By adding a few number of transistor the delay time at the latch has been comparatively reduce. As a result in the modified design the power is saved and can be used for high speed ADCs design.

CLOCK REGENERATIVE COMPARATORS

Clock regenerative comparator are widely use in design of ADCs of high speed as these type of comparator makes fast decision due to the presence of feedback(positive) in the latch stage. There are many analysis which investigate the behavior of the comparator from many respect such as random decision error[10],offset voltage[8],[9], noise[7] , kick-back noise[11]. The the above section the

analysis of delay is presented. the delay of the conventional dynamic and conventional double-tail comparator are verified and based on the above proposed comparator will be presented

I. CONVENTIONAL DYNAMIC COMPARATOR

Conventional dynamic comparator is widely used dynamic comparator for the design of analog to digital comparator .It has rail-to-rail output swing ,high input impedance , zero static power consumption. the schematic of conventional dynamic comparator is shown in fig 1.1 and fig 1.2 shows the transient simulation of conventional dynamic comparator .

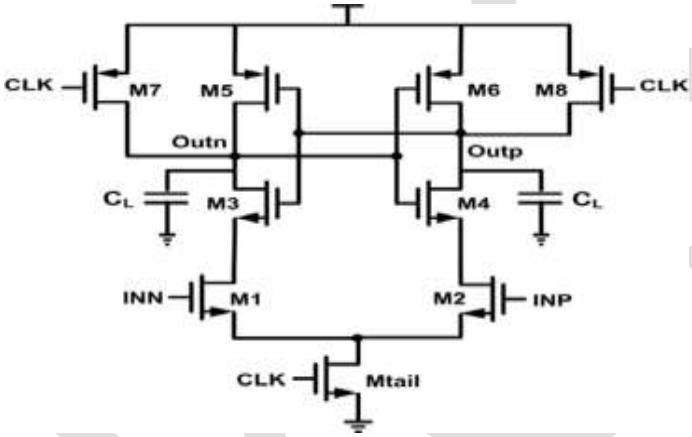

fig 1.1. Schematic of conventional dynamic comparator

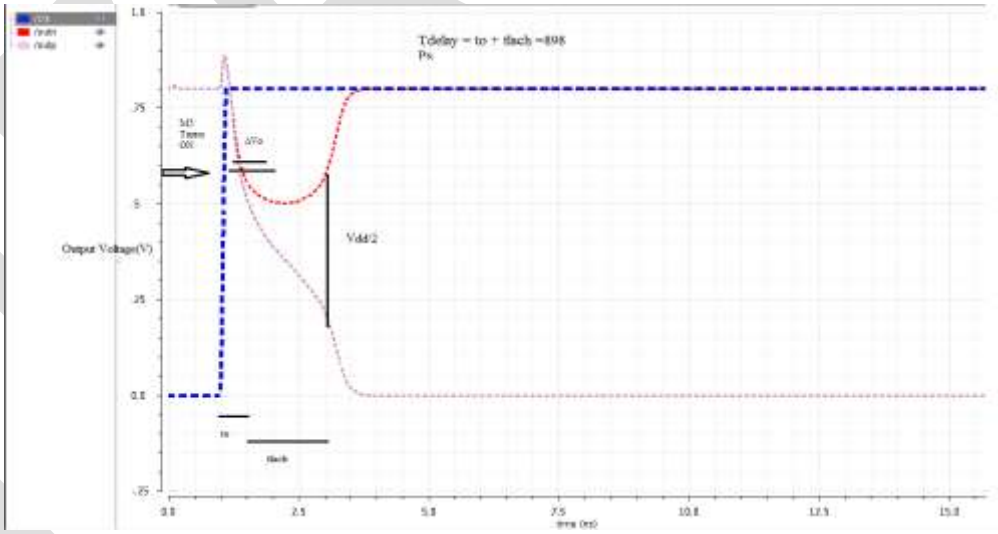

fig 1.2 :- Transient simulation of the conventional dynamic comparator for the voltage difference of 5 m V, V cm=0.7 and supply voltage of 0.8V

The delay of the above comparator consists of two delay t_0 and t_{latch} where t_o discharging delay of the load capacitance C_L and t_{latch} is the latching delay of the cross coupled inverter and hence the total delay(t_{delay}) of the above comparator is given as

$$t_{delay} = t_0 + t_{latch} = 2\frac{C_L |V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4 |V_{thp}| \Delta V_{in}} \sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right). \quad (1)$$

Where C_L is the load capacitance, $|V_{thp}|$ is the threshold voltage of M2 transistor , $g_{m,eff}$ is the transconductance of the back-to-back inverter , V_{DD} is the supply voltage ,I_{tail} is the current of the M_{tail} transistor. $\beta_{1,2}$ is the current factor of the input transistor , Δ Vin is the input voltage difference. According to equation (1) the delay of the above comparator depends directly to the load capacitance(C_L) and inversely to input difference voltage (Δ Vin) .

The main advantage of the above architecture are rail-to-rail swing at the output, better robustness against noise and mismatch, static consumption is zero. The power plot of the conventional dynamic comparator is shown in fig 1.3 and the layout of the above comparator is shown in fig 1.4

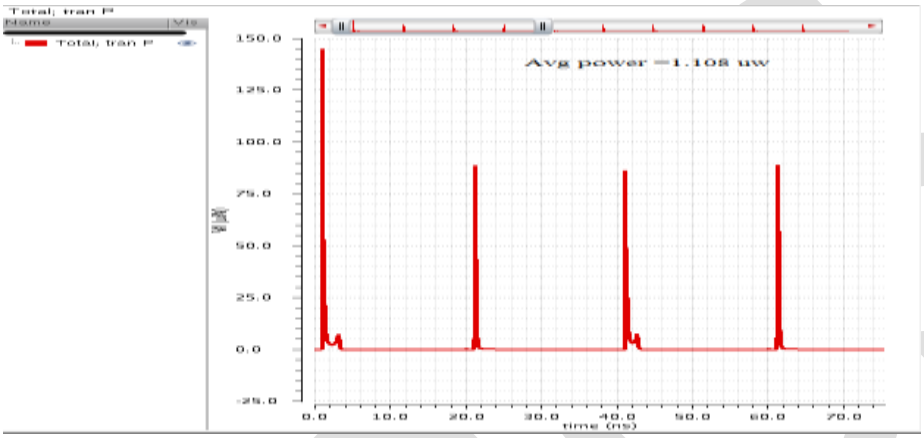

Fig 1.3 power plot of conventional dynamic comparator

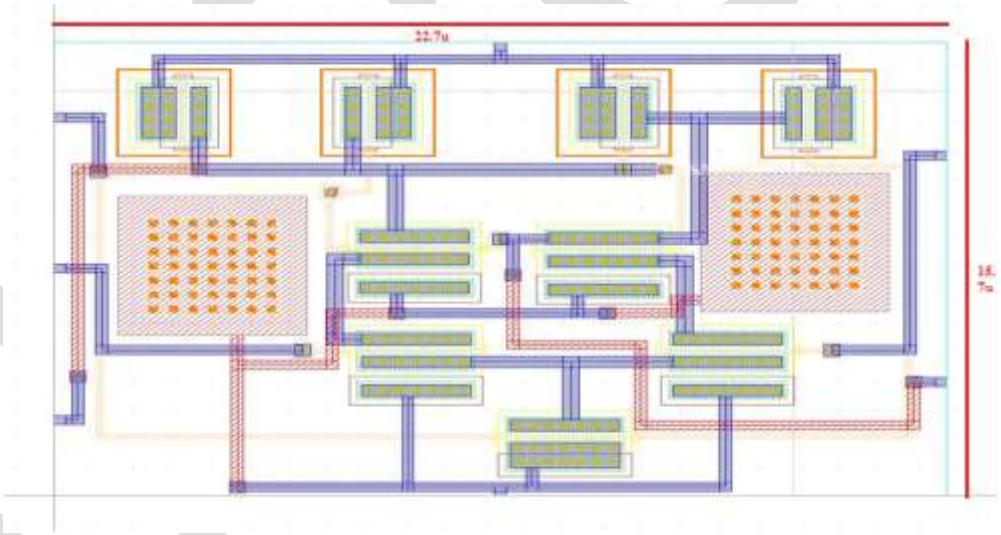

Fig 4 Layout schematic of the conventional dynamic comparator

II. CONVENTIONAL DOUBLE-TAIL DYNAMIC COMPARATOR

The schematic of double-tail dynamic comparator is shown in fig 1.5 as the above topology has large number of transistor and has less stacking and operation can be done at lower supply voltage compared to the earlier design of conventional dynamic comparator. As in these structure due to the presence of two M_{tail} transistor it provides large current at the latching stage and wider M_{tail2} requires for fast latching which is independent to V_{cm}(common mode voltage at input) and has small current at the input stage , required for low

offset[6]. The fig 1.6 shows the transient simulation of the conventional double-tail dynamic comparator for input voltage difference of ΔVin=5mv , V_{cm}=0.7v and V_{DD} = 0.8V

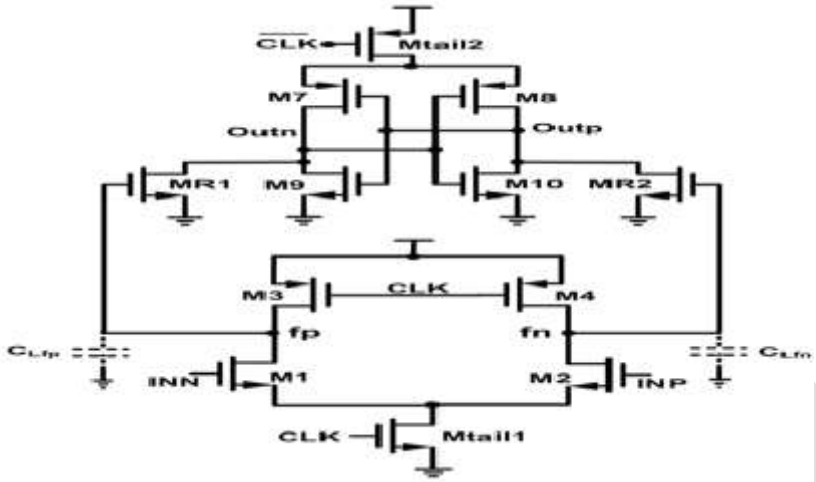

fig 1.5 Schematic of conventional double-tail dynamic comparator

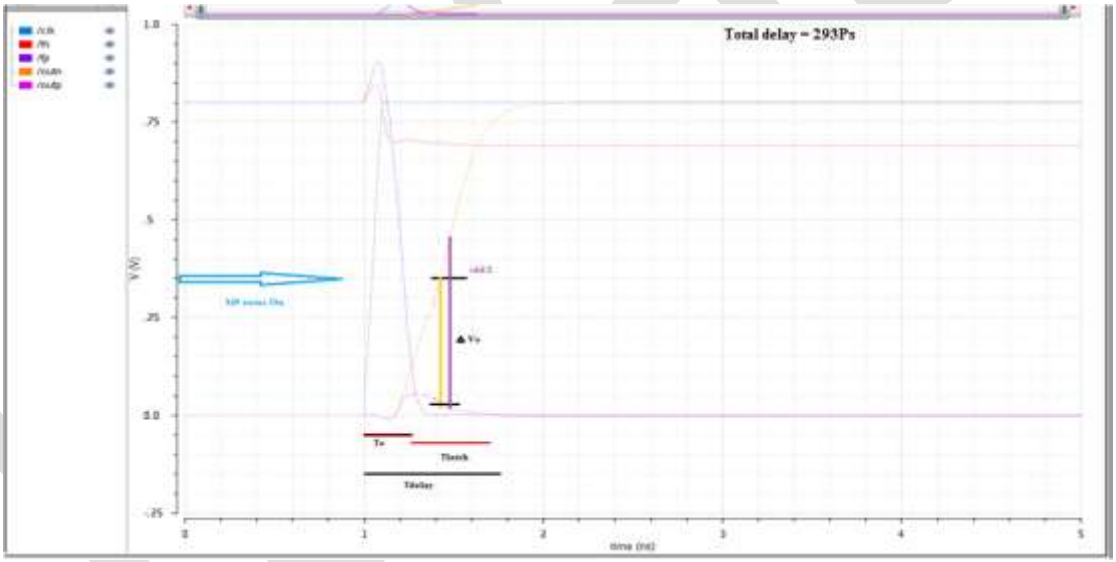

Fig1.6 Transient simulation of the conventional double-tail dynamic comparator for input voltage difference of ΔVin=5mv ,V_{cm}=0.7v and V_{DD}

The delay of the double-tail dynamic comparator comprises of two delay t_0 and t_{latch} . which is similar to that of conventional dynamic comparator . Here t_0 is the capacitive charging of the capacitance at the load C_{Lout}(at the out*n* and out*p*) until the transistor (M9/M10) are on, and hence the latch regeneration starts and t_0 is determined. The total delay of the above comparator is given as

$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$
$$= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD} \cdot I_{tail2}^2 \cdot C_{L,fn(p)}}{8V_{Thn}^2 \cdot C_{Lout}g_{mR1,2}g_{m1,2}\Delta V_{in}}\right).$$

where $g_{mR1,2}$ is transconducatance of the transistor(M_{R1} and M_{R2}) , $I_{tail\ 2}$ is the current of M_{tail2} transistor , Δ Vin is the voltage difference at the input , ΔV_0 is the output voltage difference. The fig 8 and fig 1.7 below shows the power plot for calculating power and layout for determining area respectively of double tail dynamic comparator.

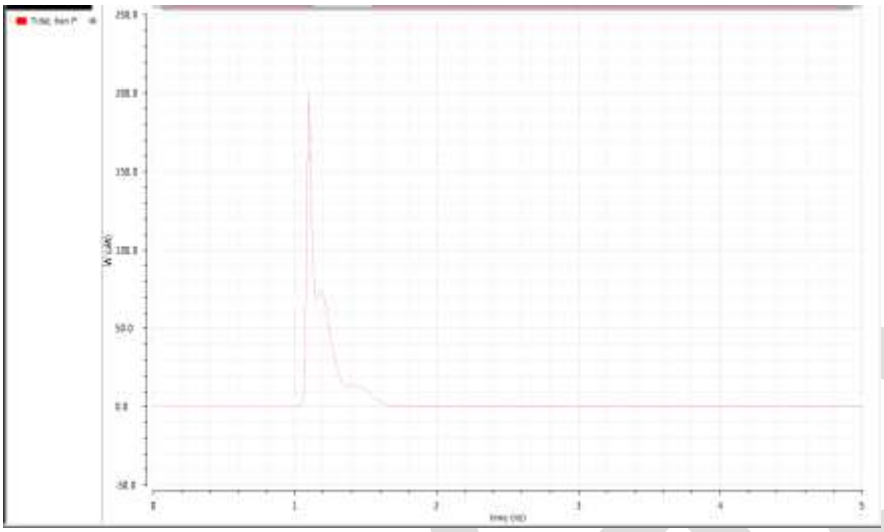

Fig 1.7-Power plot of double-tail dynamic comparator

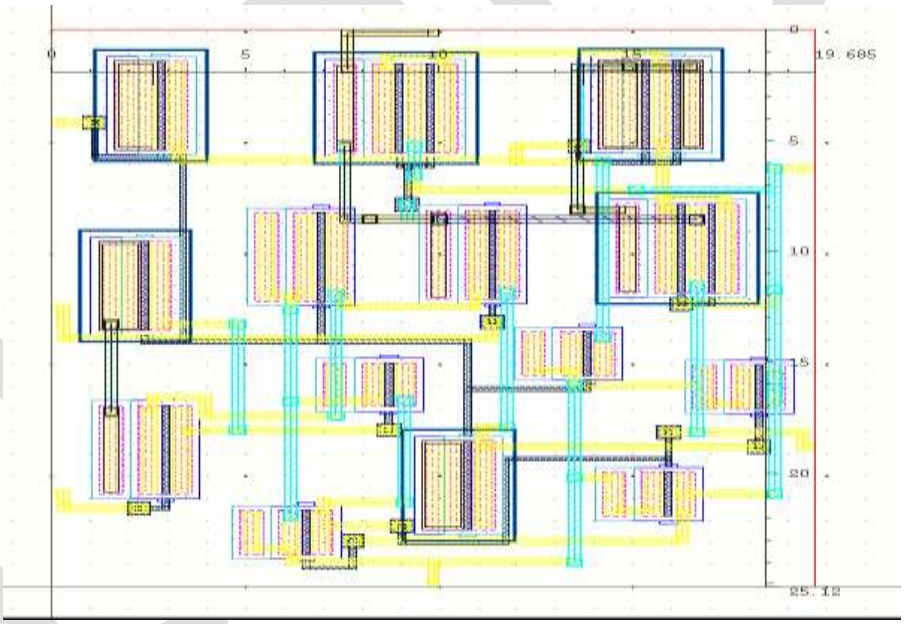

Fig 1.8 - Layout of double tail dynamic comparator

III PROPOSED DOUBLE TAIL DYNAMIC COMPARATOR

The schematic of proposed design is compared with double-tail dynamic comparator is shown in fig 1.9 . In the proposed design the lower input state is replace by differential amplifier with PMOS load

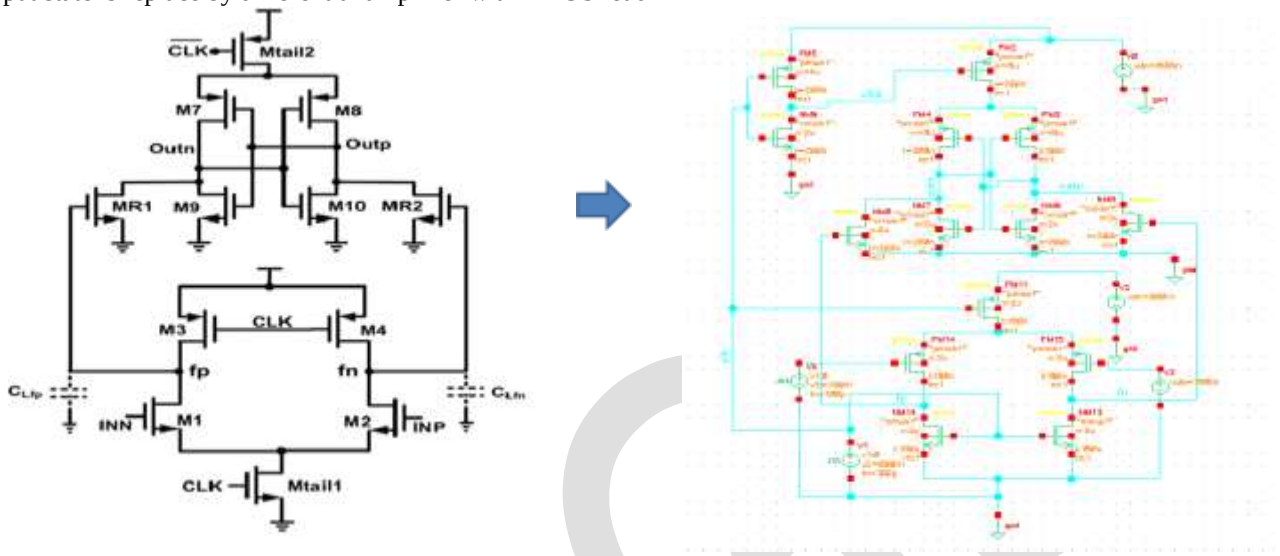

Fig :- 1.9 Schematic of proposed comparator(right) with double-tail dynamic comparator(left)

The delay of the proposed double-tail dynamic comparator is comparatively reduced in comparison to double-tail dynamic comparator. The power plot and Transient simulation of the proposed double-tail dynamic comparator for input voltage difference of $\Delta Vin=5mv$, $V_{cm}=0.7v$ and $V_{DD} = 0.8V$ is shown in fig 2.1 and fig 2.2 shows the layout of proposed double-tail dynamic comparator

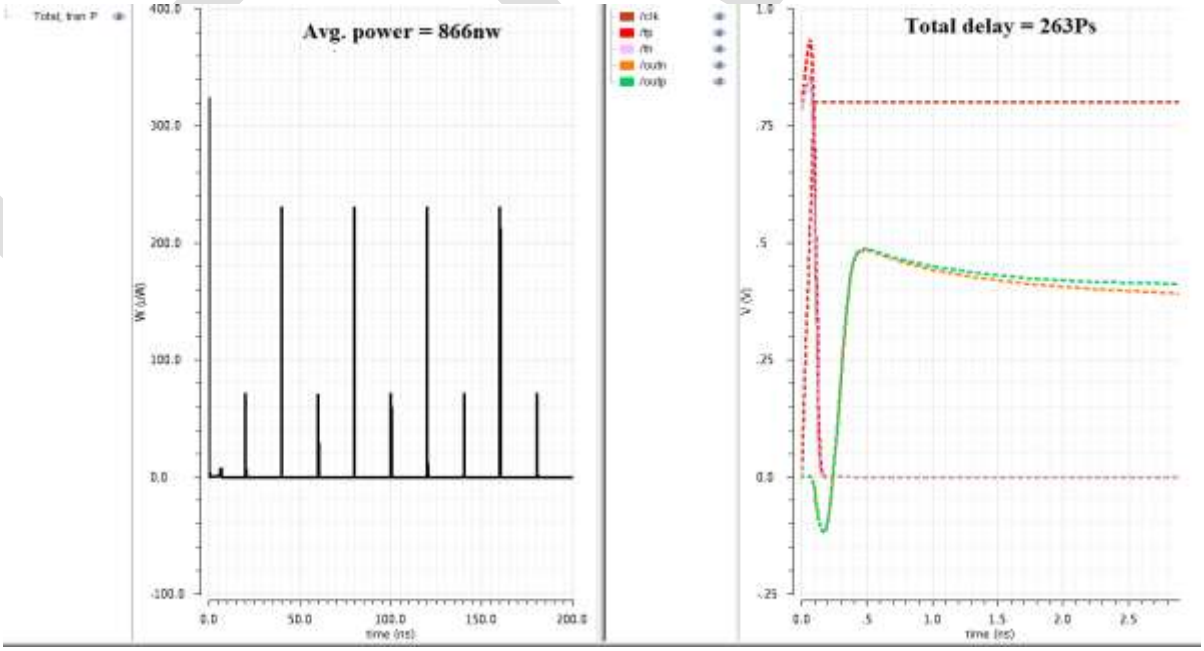

Fig 2.1 :- Power plot and Transient simulation of the Modified double-tail dynamic comparator for input voltage difference of $\Delta Vin=5mv$, $V_{cm}=0.7v$ and $V_{dd} = 0.8V$

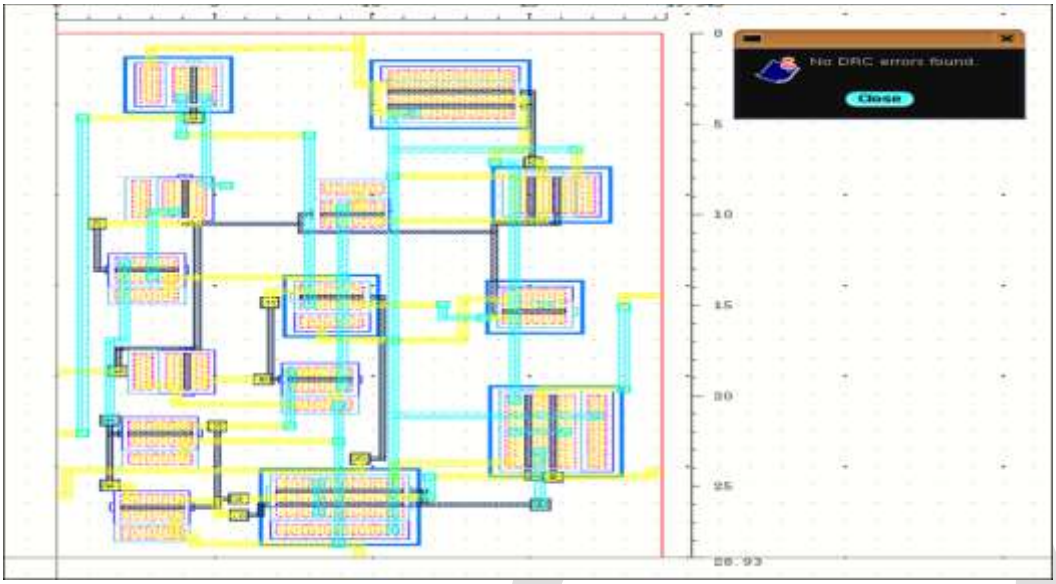

fig 2.2 Layout of proposed double-tail dynamic comparator in 180nm technology

SIMULATION RESULT

The comparison table has been presented to compare the results of proposed comparator with conventional and double-tail dynamic comparators. the above circuit are simulated in a 180nm CMOS technology

Comparator Structure	Conventional Dynamic Comparator	Double-tail Dynamic Comparator	Proposed Double-tail Dynamic Comparator
No of Transistors used	9	14	16
Supply Voltage (V)	0.8	0.8	0.8
Delay(Ps)	898.2	293	263
Energy (FJ)	1.108µ	2.125 µ	866 n
Estimated Area	22.7µ * 15.7µ	28µ*13µ	28.9µ*19.5µ

CONCLUSION

A new proposed double-tail comparator shows better performance as compared to conventional dynamic and double-tail dynamic comparator. As it is shown that the delay of the proposed design is 263 Ps which is comparatively lesser than the earlier also energy per conversion is reducing from 1.108µ in conventional dynamic to 866 ns in proposed double-tail. The proposed double-tail dynamic comparator can be used for the design of high speed ADCs as the delay is reduced and hence the operation will be faster. As in the proposed structure the number of transistor is more so the area of the design is more which is one of the disadvantage of the above comparator

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