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A Strategical Description of Ripple Borrow Subtractor in Different Logic Styles

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ABSTRACT – The demand and popularity of portable electronics is driving designers to strive for small silicon area, higher speeds, low power dissipation and reliability. Design of 2-input AND, 2-input OR, 2-input XOR and an INVERTER, which are the basic building blocks for the 4- bit Ripple borrow subtractor. This paper thoroughly involves designing of ripple borrow subtractor in cMOS logic, transmission gate logic and pass transistor logic styles. The schematic design is further transferredto prefabrication layout. Simulation of the microwind layout realizations of the subtractor is performed and results are discussed. From the results obtained comparison of cMOS logic, transmission gate logic and pass transistor logic is done and discussing the efficient logic for ripple borrow subtractor.

Keywords— cMOS logic, transmission gate logic, pass transistorlogic, fullsubtractor, ripple borrow subtractor.

INTRODUCTION

In thispaper,we have presenteda brief review on Rippleborrow subtractorusingcMOS,Transmission gatesandPasstransistorlogic style.Thebasiccircuitdiagramof 1 bit Fullsubtractoris asdescribedbelowalongwiththe blockdiagram andits truthtable. Full subtractor is a combinational circuit which is used to perform subtraction of three bits, it has three inputs a(minuend) and b(subtrahend) and borrow_in(subtrahend) and two outputs d(difference) and borrow_out(borrow).

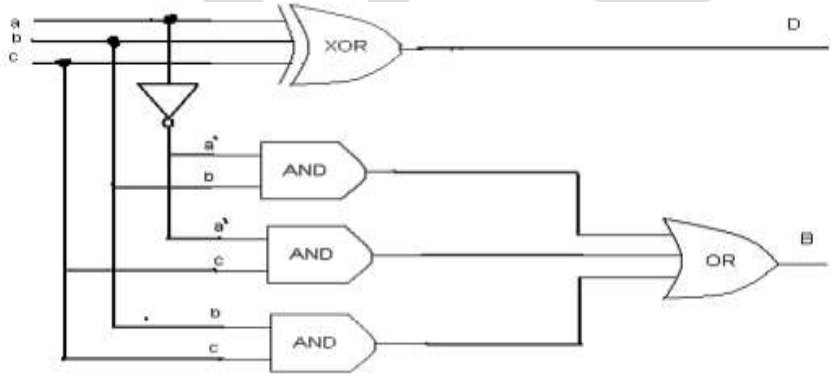


Fig. 1. Gate level representation of full subtractor

a_i	b_i	bor_i	$diff_i$	bor_{i+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

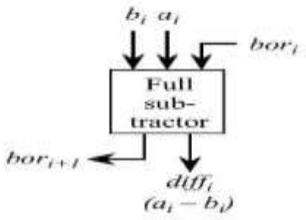


Fig. 2. Truth table and block diagram of full subtractor

CIRCUITTECHNIQUES

FULLSUBTRACTOR

Thefull-subtractorcircuitsubtractsthreeone-bitbinary numbers(A,B,borrow_in)andoutputstwoone-bit binary numbers,a difference(D)anda borrow(borrow_out).

RIPPLE BORROW SUBTRACTOR

It is possible tocreate logicalcircuit usingmultiplefullsubtractortosubtractN(precase4)bitnumbers. Eachfullsubtractorinputsaborrow_in(borrow input)whichistheborrow_out (borrow output) of previoussubtractor.Thiskindofsubtractorisripple borrow subtractorsince eachborrowbitripples tothenextfullsubtractor

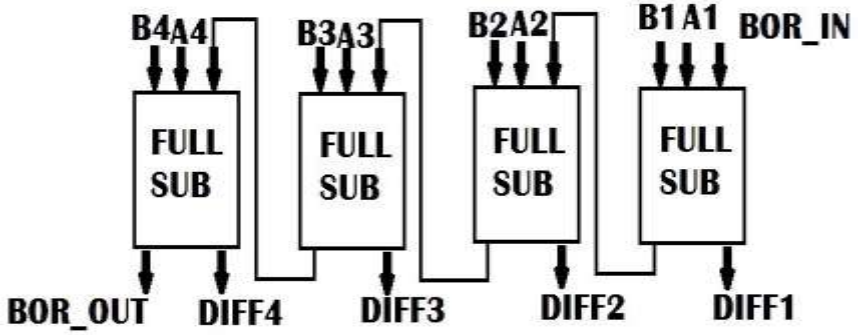


Fig. 3. Ripple borrow subtractor

4-BITRIPPLEBORROW SUBTRACTORUSINGCMOSCIRCUITS

cMOS is referred to as complementarysymmetry metaloxide semiconductor (COS-MOS).Thewords “complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. The circuit level description of the Ripple Borrow Subtractor in cMOS logic is described below.,

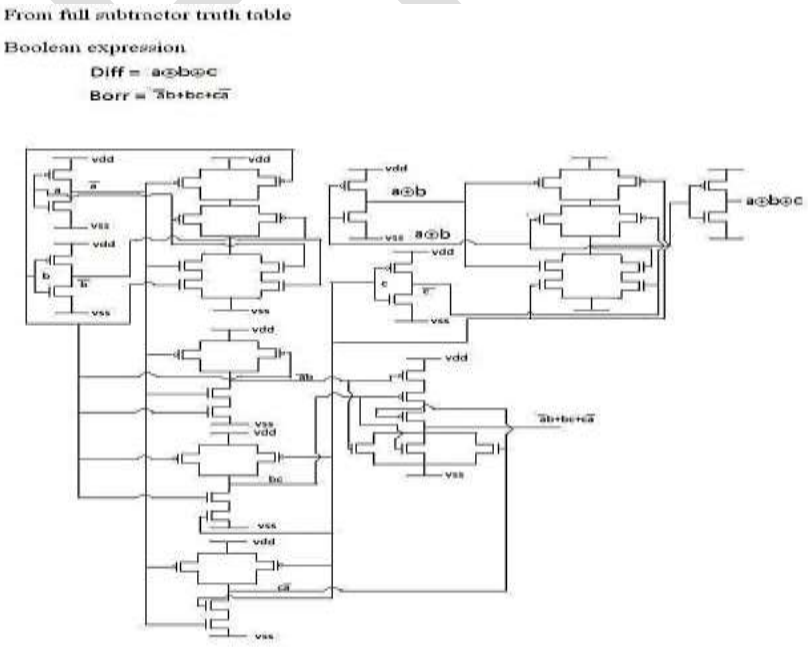


Fig. 4. Ripple borrow subtractor in cMOS logic.

4-BIT RIPPLEBORROW SUBTRACTOR USING TRANSMISSIONGATES

TheCMOStransmissiongateconsistsoftwoMOSFETs,one n-channelresponsibleforcorrecttransmissionoflogiclow,and one p-channel, responsibleforcorrecttransmissionof logic high.The circuit level description of the Ripple Borrow Subtractor in Transmission Gate logic is described below.

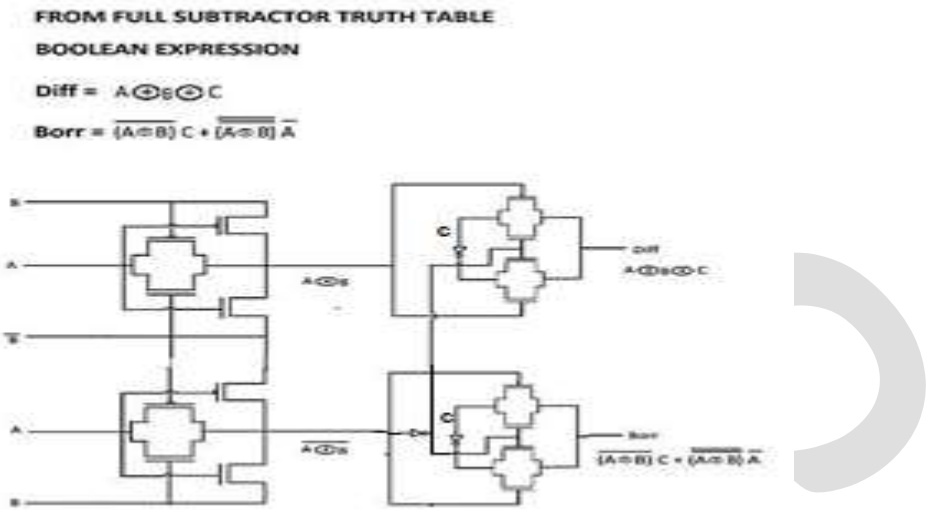


Fig. 3. Ripple Borrow Subtractor in Transmission Gate Logic.

4-BIT RIPPLEBORROW SUBTRACTOR USINGPASS TRANSISTORS

Wecanview thecomplementaryCMOSgateasswitchingthe output pintooneof powerorground.A slightlymore general gateisobtainedifweswitchtheoutputtooneofpower; ground;orany oftheinputsignals.Insuchdesignsthe MOSFETis consideredto be a passtransistor.When used as a passtransistorthe devicemay conductcurrentineither direction.The circuit level description of the Ripple Borrow Subtractor in Pass Transistor logic is described below.,

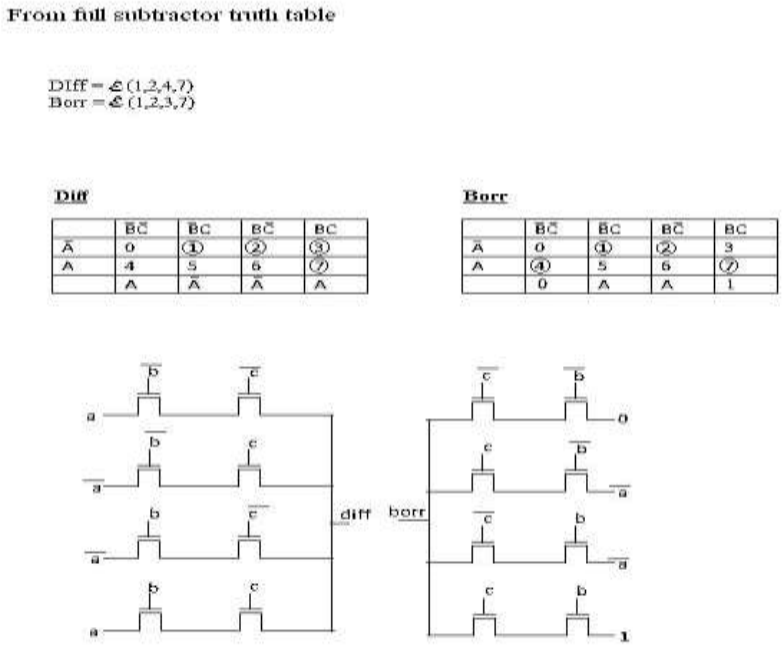


Fig. 4. Ripple Borrow Subtractor in Transmission Gate Logic.

DESIGN ANDLAYOUT ASPECTS

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING cMOS LOGIC

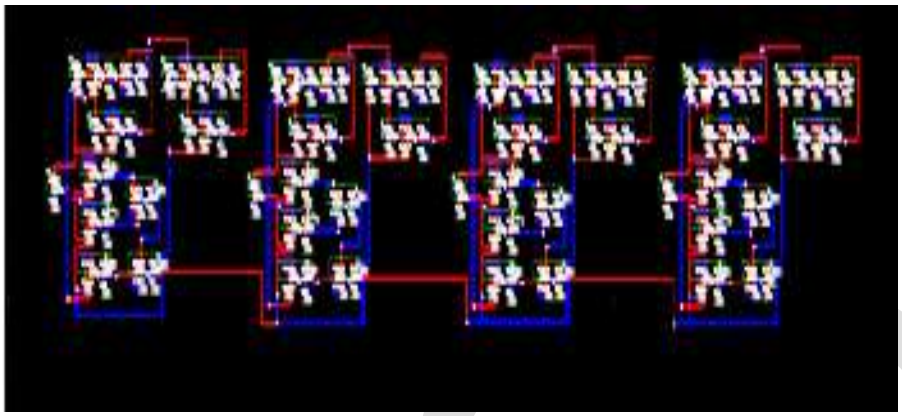


Fig. 5. Layout of ripple borrow subtractor using cMOS logic

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING TRANSMISSION GATE LOGIC

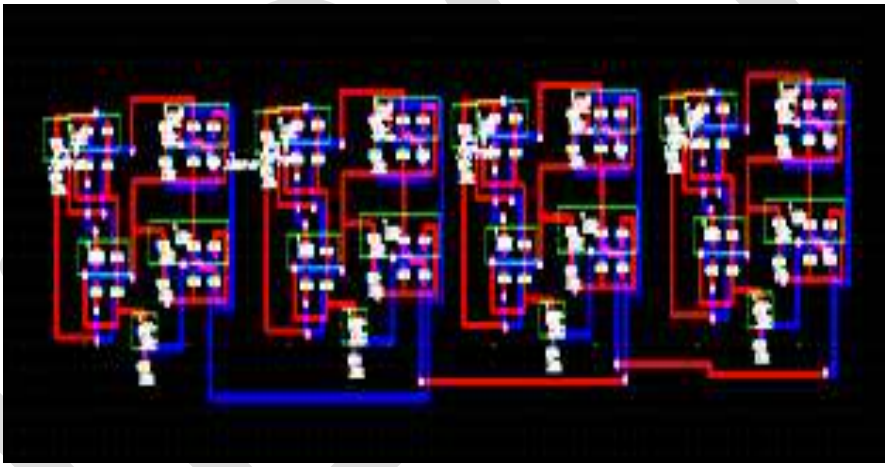


Fig. 6. Layout of ripple borrow subtractor using transmission gate logic

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING PASS TRANSISTOR LOGIC

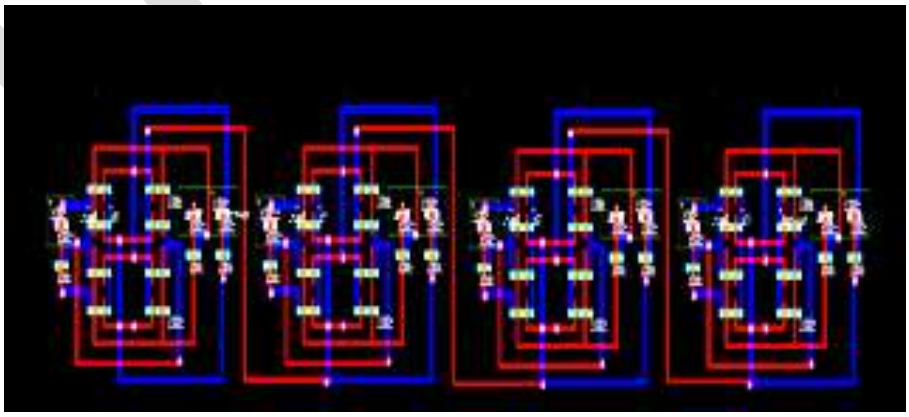


Fig. 7. Layout of ripple borrow subtractor using pass transistor logic

SIMULATIONAND RESULTS

SIMULATION OF RIPPLE BORROW SUBTRACTOR USING cMOS LOGIC

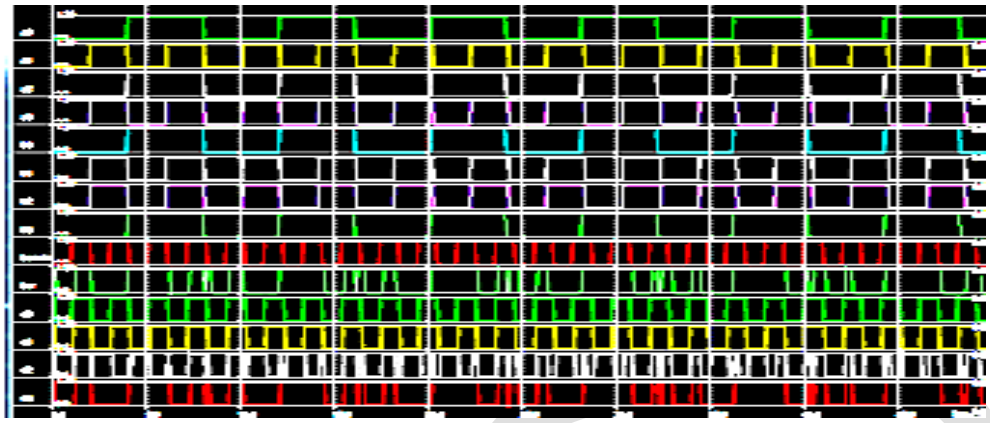


Fig. 8. Simulation of ripple borrow subtractor using cMOS logic

SIMULATION OF RIPPLE BORROW SUBTRACTOR USING TRANSMISSION GATE LOGIC

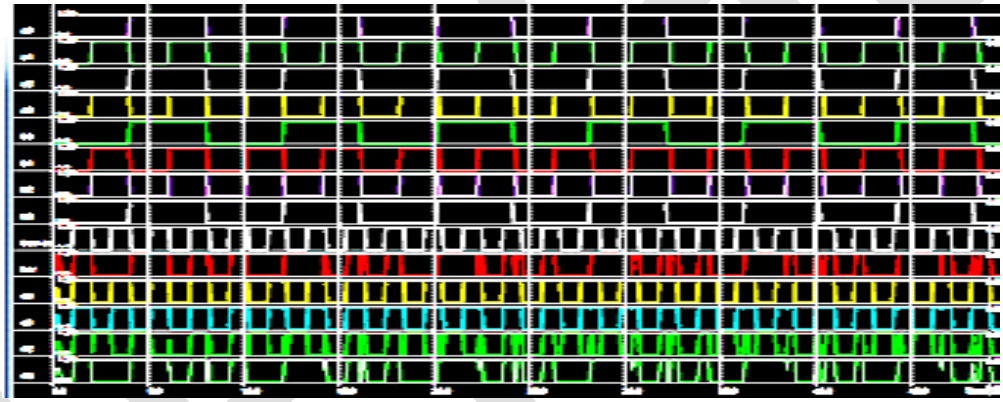


Fig. 9. Simulation of ripple borrow subtractor using transmission gate logic

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING PASS TRANSISTOR LOGIC

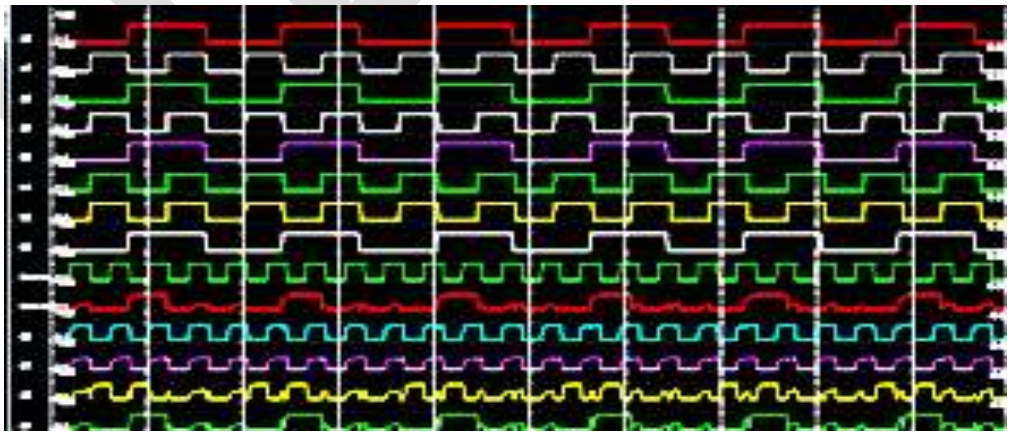
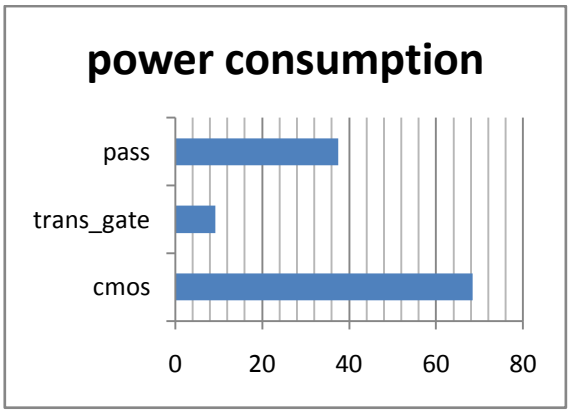


Fig. 10. Simulation of ripple borrow subtractor using pass transistor logic

POWER ANALYSIS

Thetable showstheresultsof4-bitrippleborrow subtractorusing cMOS circuits, TransmissiongatesandPassTransistors.Itcomparesthesecircuitsregarding Power consumption.Fig.11 representstheaboveresults graphically.



CIRCUITS	POWER CONSUMPTION
CMOSCIRCUITS	68.356uW
TRANSMISSIONGATES	9.225uW
PASSTRANSISTORS	37.515uW

Fig. 11. Power consumption.

CONCLUSION

In this paper, an attempt has been made to design 2input AND, 2inputOR, 2inputXOR,whichare the basicbuilding blocksforthebenchmarkcircuits4-bitRippleborrow subtractor. Theproposedcircuitshaveofferedanimprovedperformance inpower dissipation.Inthispaper,we canbe concludedthatasthepowerdissipationof transmission gatecircuitsis muchlessthanthepowerdissipationofcMOSandPasstransistors,thusitprovestobemuchefficientthan the circuits from cMOSandPass transistors.The circuitandits VLSItechnologyisveryusefulinthe applications relatedtorural developmentas itislesspower consumingandthuscanbeefficiently usedinvarious technologies.

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